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Microgripper force feedback integration using piezoresistive cantilever structure

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Microgripper Force Feedback Integration Using Piezoresistive Cantilever Structure

by

Todd R. Simon

A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical Engineering.

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Abstract

Force feedback is an important feature in most microgripper applications, but it is commonly overlooked. To successfully implement this feature, a cantilever structure has been designed and fabricated to integrate force feedback into a microhand gripper. The piezoresistive properties of doped polysilicon are used to transduce the mechanical stress of an object pressing against the cantilever sensor, resulting in a change in resistance or voltage capable of being monitored with external hardware. The force sensing structure was designed to have a fabrication process compatible with that of the microhand, allowing for their eventual integration. This fabrication process uses both bulk and surface micromachining techniques to create the cantilever structure, a balloon actuator (utilized in the microhand), and the interconnect to interact with both the electrical sensors and the pneumatic actuators. The prototype fabrication successfully defined the majority of the MEMS device with the exception of the final step. The release of the cantilever failed due to underetching of the entire device rather than just the cantilever, which was desired. Recommendations to solve this problem and improve the fabrication process are presented.

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List of Abbreviations

ADC	Analog-to-Digital Converter
AFM	Atomic Force Microscopy
APM	Ammonia hydroxide-hydrogen Peroxide-water Mixture
ASM	Advanced Semiconductor Materials
BOE	Buffered Oxide Etch
CVD	Chemical Vapor Deposition
DI	DeIonized
GF	Gauge Factor
HMDS	HexaMethylDiSilazane
HPM	Hydrochloric acid-hydrogen Peroxide-water Mixture
IC	Integrated Circuit
K&S	Kulicke & Soffa
LTO	Low Temperature Oxide
MEMS	MicroElectroMechanical Systems
MIS	Minimally Invasive Surgery
PCB	Printed Circuit Board
PDS	Parylene Deposition System
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PR	PhotoResist
PVD	Physical Vapor Deposition
RCA	Radio Corporation of America
SC1/2	Standard Clean 1/2
SCS	Specialty Coating Systems
SMA	Shape Memory Alloy
SNR	Signal-to-Noise Ratio
SRD	Spin, Rinse, and Dry
SVG	Silicon Valley Group
TMAH	TetraMethylAmmonium Hydroxide
UV	UltraViolet
VDP	Vapor Deposition Polymerization

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1 Introduction

1.1 Background

Microelectromechanical systems (MEMS) are devices and integrated systems comprised of micro-scale sensors, actuators, and electronics using technology developed from the integrated circuit (IC) industry. This technology includes chemical and physical vapor deposition, lithography, wet and dry etching, and thermal processes. Thin films of metals, semiconductors, and insulators can be applied to a substrate using vapor deposition. Lithography allows for transference of a pattern onto a substrate by exposing photoresist to UV light passed through a mask of the desired pattern. The portion of a positive photoresist exposed to the light will develop away, leaving a copy of the pattern in the mask on the wafer. In etching processes, removal of material chemically and/or abrasively allows the transference of the pattern from the photoresist to the wafer. Thermal processes diffuse impurities (dopants) in order to change resistivity and other properties. Exposure to high temperature environments can also grow films. Through numerous iterations of these processes, MEMS devices can be fabricated to meet the needs of many diverse applications.

MEMS has become a very popular solution to many of today's problems including: national security [1], video game interfaces [2], automotive sensors [3,4], and medical devices [5,6]. One particular use of MEMS has been minimally invasive surgery (MIS). MIS has a number of advantages over customary surgical procedures

as it decreases trauma induced in the patient by requiring smaller access incisions. This corresponds to reduced pain, quicker recovery times, and better cosmetic results. For example, during open-heart surgery the rib cage is split in the process of giving access to the heart; this predictably requires a longer and more expensive hospital stay than if the rib cage could be left intact. MIS allows for smaller incisions by using special surgical instruments and endoscopes to reach the site of the operation and perform the necessary procedures. Unfortunately, these instruments remove some of the feedback available to surgeons during traditional operations, as their only means of observing MIS operations is through the endoscope. They therefore lose the tactile/haptic responses provided by their hands, the stereo vision of their eyes, and the perspective and degrees of freedom provided by an open cavity. Without tactile feedback the surgeon loses important information such as how hard he or she is pulling and cutting. They also lose textural acuity that can inform them about what they are touching. Without certainty about what they are touching, they could inflict damage unexpectedly, such as cutting a nerve or blood vessel. Ferreira and Mavroidis explain the importance of force feedback in the application of grippers, which is the primary application of this thesis [7].

> *The lack of direct 3-D vision feedback from the n-world and the fragility of the telemanipulated n-objects make real-time force feedback an absolute necessity of the macro-/n-world interface. Indeed it is fundamental to the understanding of the condition of the gripper during operation. An excessive force applied on an n-object may lead to a nonnegligible degree of probe or object deformation and may destroy the n-object or make it flip away.*

Although this passage is referring to nanoscale (n-)objects, it is no less true for the microscale world.

According to Rebello [8], MEMS can overcome some of the disadvantages of MIS: "MEMS technology can improve surgical outcomes, lower risk, and help control costs by providing the surgeon with real-time data about instrument force, performance, tissue density, temperature, or chemistry, as well as provide better and faster methods of tissue/fluid preparation, cutting, and extraction." This real-time data is feedback allowing the surgeon to be more confident in what he or she is doing, and thereby produce better results. Additionally, MEMS brings new means of actuation to MIS allowing for more precise actuation. Strain gauges can give the necessary feedback to perceive the elastic properties of what is being gripped, overcome the problems of instrument force, and sense the pulsation of microvessels [9]. Similarly, pressure sensors can give insight into the type of material surrounding an instrument. Exposed electrodes can check the impendence of a material or pick up electrical signals from nerves. Verimetra, Inc. has come up with a product to integrate many of these MEMS features into a smart scalpel (Figure 1-1). Ultrasonic sensors [10,11] and optical MEMS [12,13] can assist in imaging the instrument surroundings. Micromotors driven by piezoelectrics [14] can give better control over precision movements. Actively steerable catheters, using Shape Memory Alloy (SMA) technology, can improve navigation and vantage point [15,16,17]. Clearly, MEMS devices offer a very wide range of solutions to MIS problems.

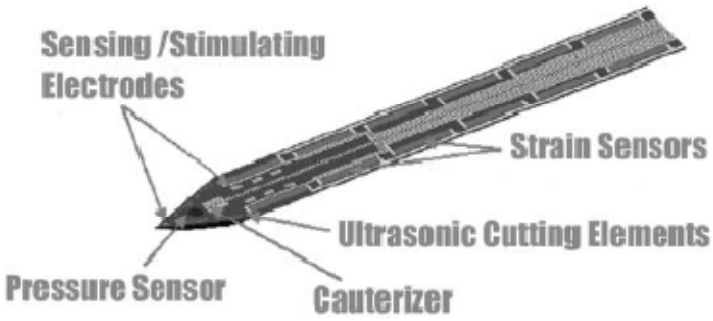


Figure 1-1: Data Knife smart scalpel by Verimetra, Inc. Reprinted with permission [8]. © 2004 IEEE

1.2 Basic Goal

This project attempts to provide force/pressure feedback by using MEMS to improve the functionality of the microhand in Figure 1-2 [18]. Similar devices have been developed in the past [9,19,20,21,22,23,24], but are more rigid and only grip on two sides (Figure 1-3) rather than encapsulating a particle, making them less effective in biological settings. The process developed here endeavors to be compatible with the fabrication process of the microhand, and allowing the designs to be combined into one device, not requiring assembly after separate fabrications. Rebello indicates that integration is important because attaching a sensor to a surgical tool post-production introduces additional sources of error, limits system size, and limits the capabilities of the technology [8]. The final goal is to improve the functionality of the microhand by allowing a computer system to assist in operations and providing haptic feedback to the user.

By working with only biocompatible materials, certification for MIS applications should be easier. The materials (silicon and its derivatives) and the processes used to form traditional MEMS devices are generally biocompatible and

not harmed by a number of sterilization procedures [25]. Similarly, Parylene is marketed as a biocompatible material [26]. The only bioinncompatible material in this process is the aluminum. However, it can be encapsulated in a Parylene coating.

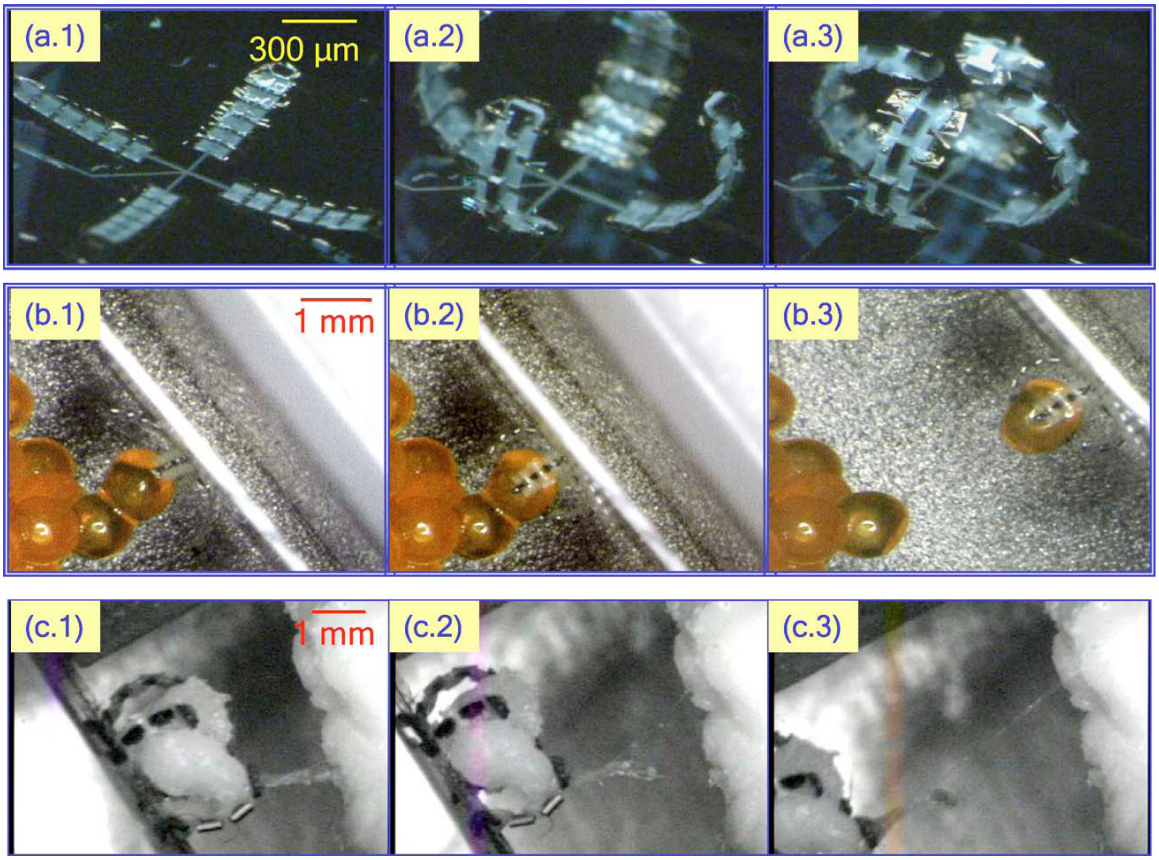


Figure 1-2: Microhand demonstrating its ability to flex into different positions (a) and manipulate different biological materials: capelin eggs (b) and fatty tissue found in the stomach of a swine (c). Reprinted with permission from [18]. © 2006, American Institute of Physics.

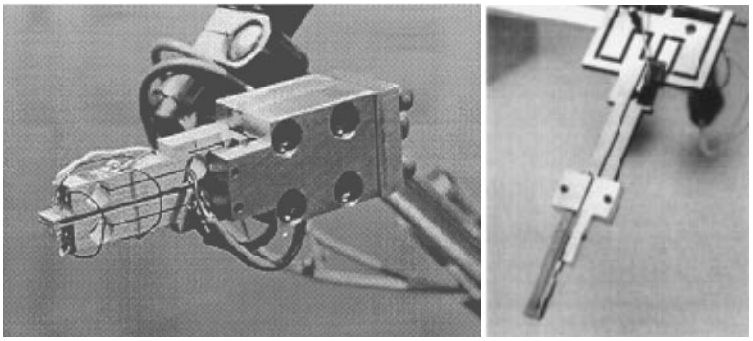


Figure 1-3: Examples of microgrippers with integrated force sensors (left, [19], © 1999 Cambridge University Press, reprinted with permission of Cambridge University Press) (right, [21], © 1998 IEEE, reprinted with permission).

1.3 Outline

The organization of this thesis is as follows: Chapter 2 will cover the design of the sensor (Figure 1-4) and underlying theory. Chapter 3 details the process used to fabricate the sensor and the purpose of each step. Chapter 4 reports and discusses observations made during fabrication and potential solutions for problems encountered. Conclusions and recommendations for further work are offered in Chapter 5.

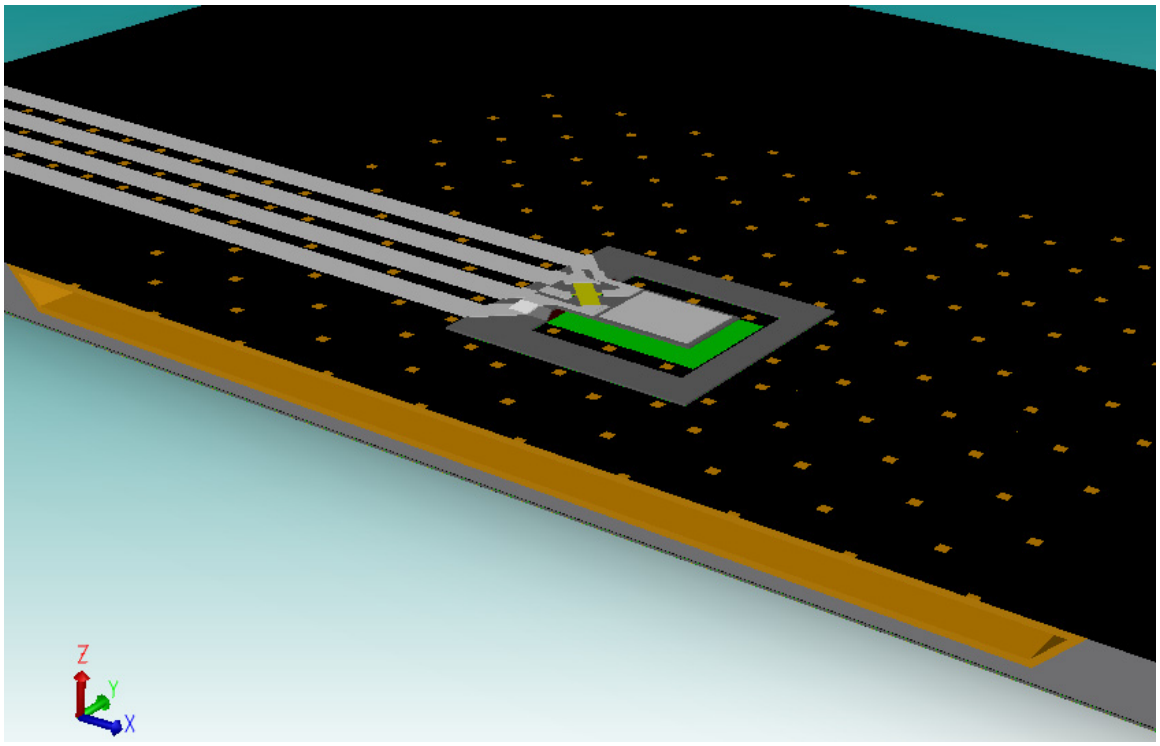


Figure 1-4: Force sensor for microgripper integration: cantilever structure (grey) with piezoresistive transducer (yellow) on balloon actuator (orange), as simulated in ConventorWare.

2 Theory & Design

2.1 MEMS Force Sensing Mechanisms

Numerous mechanisms for sensing force have been developed in the past. The following discussion details the methods that were thought to be candidates for use in this application. Other methods were disregarded on the basis that the mechanism had to be contained within the device. In this vein, optical means of observing deflection, such as measuring the displacement of a laser beam bouncing off a deflectable beam, are problematic. Mechanisms that transduce by altering an RF field were also deemed impractical, as they would not allow multiple sensors to be concentrated in one area.

2.1.1 Capacitance

Sensors operating on the capacitive mechanism rely on two conductive plates separated by an insulator, effectively forming a capacitor. Traditionally, one of the plates is held fixed as the other moves in response to an external force or pressure. As the plates move together, the capacitance increases according to

$$C = \frac{\varepsilon A}{d} \tag{2-1}$$

where C is the capacitance; ε, the dielectric permittivity of the insulator; A, the cross-sectional area shared by the plates; and d, the distance between the plates. However, the range of variation that can reasonably be expected from such sensors is in the femto-farad range, which is easily lost in the noise of interconnect. A way to overcome this would involve on-device electronics to convert the capacitance

variation into a frequency variation with a simple oscillator circuit, or some other more robust signal. However, the on-device electronics would require many additional processing steps and add complexity to the overall system.

2.1.2 Piezoelectric

Piezoelectric materials have a unique property in which the application of mechanical strain induces an electric field and *vice versa*. This unique property allows for both actuation and sensing. Mechanically, such a sensor would be a simple stack of layers of such materials protruding above the surface. Contact with an object would compress the stack, giving rise to a measurable voltage. (The stack serves to multiply the effects of an individual layer of piezoelectric material.) However, the charge displaced by the creation of this electric field is rather minimal and, although measurable, it dissipates reasonably quickly due to the finite resistance in the measurement systems and environment. Additionally, the materials that exhibit this property, such as lead zirconate-titanate (PZT), cannot be easily integrated in a MEMS/CMOS process.

2.1.3 Piezoresistive

Piezoresistive materials respond to mechanical strain with a change in resistivity. This simple effect is conveniently present in silicon, the ubiquitous material in the microelectronic industry, lending itself well to MEMS. Piezoresistivity results from changes in the position of atoms in a material that has a corresponding impact on the energy bands of the material [27]. This minor shift in energy bands influences the ease with which electrons flow through the material for

a given voltage, therefore causing a slight change in the material's resistance. Additionally, strain alters the dimensions of the resistor and that has an impact on resistance. For instance, if stress is applied along the length of a material it will elongate and the width of the resistor will shrink according to Poisson's ratio, increasing resistance. These two effects can be summarized with gauge factor (GF), which predicts the net resistance change according to

$$\frac{\Delta R}{R} = \varepsilon \, GF \qquad \textbf{(2-2)}$$

where $\frac{\Delta R}{R}$ is the percent change in resistivity and ε is the mechanical strain applied. Because strain affects resistance differently depending on the orientation of its application, there are different GF coefficients for strain applied parallel (||) and perpendicular (⊥) to current flow in the resistor, as conveyed in Table 2-1. This table also indicates a dependence on doping, which is logical since the atomic composition will change the energy bands and the elements used for N and P-type doping are different. Furthermore, dopant concentration also has an impact as demonstrated by the variance across doping dose.

Table 2-1: Gauge Factor in Polycrystalline Silicon at Different Implant Doses (adapted from [28])

	P-type (Boron)		N-type (Phosphorous)	
Dose (cm^{-1})	GF ‖	GF ⊥	GF ‖	GF ⊥
5.0E14	9.1	-10.3	-8.0	10.7
7.5E14	11.9			
1.0E15	20.2		-10.5	9.7
2.5E15	30.9	-9.3	-13.6	7.5
5.0E15	26.2	-8.8	-15.8	5.1

Because the change in resistance is static for an applied force, it is well suited for applications that require maintaining a constant grip over a given time period, unlike the piezoelectric sensor. Resistance is also beneficial because it is simple to measure, unlike capacitance. One way to achieve this is to change the varying resistance into an analog voltage signal using a resistor network. Finally, Singh et al. recalls that the piezoresistive properties of semiconductors, such as silicon, are quite large relative to other materials, making silicon piezoresistors an ideal choice for this application [29]. For these reasons, the piezoresistive phenomenon was chosen as the transduction scheme for this device.

2.2 Cantilever and Support Structure

Ferreira and Mavroidis [7] references a need to sense very small "forces in the range of 0.1-200 μN and more must be sensed with nano-Newton resolution." They site this range for general applications in biological and physical sciences in the nanoworld. For the first attempt at this, the range has been limited to a more modest 1 to 100 μN with only μN resolution in consideration of the complexity of even this limited goal and the integration of an actuation mechanism. Additionally, the MIS application may involve larger force than those mentioned above. However, if such small senses can be monitored, the microhand may be useful for other applications, the sensitivity can be scaled back for MIS applications, and empirical tests can be done to find the optimal sensitivity and range.

As the piezoresistive coefficients are weak and the forces to be sensed are small (1 to 100 μN), it is necessary to utilize mechanical amplification to allow the

stress to generate a measurable resistance change. Therefore, a cantilever structure has been designed. The structure is similar to that found in atomic force microscopy (AFM) for the purpose of mechanical force transduction [7]. As force is applied to the cantilever, stress forms across the beam structure causing it to deform in strain. The cantilever works like a lever in simple machines; it serves to take a small force with a large displacement and turn it into a larger force. As the beam is bent down, the top surface experiences tension and the bottom surface experiences compression. Most of the beam's bending occurs near the fixed end (the fixture point) where there is a concentration of stress and strain at the junction (Figure 2-1). Likewise, the surfaces experience the greatest stress and strain because they are furthest from the center of the beam, which is under neither compression nor tension (Figure 2-2). Placing the piezoresistor networks near the point of maximum stress increases the sensitivity of the sensor.

By tuning the width, length, and thickness, the following equation can be used to achieve a sensing range of 1 to 100 μN while maintaining maximum stress.

$$\sigma_{max} = \frac{6\,L}{W\,t^2} F = \frac{3\,E\,t}{2\,L^2}\delta \qquad \textbf{(2-3)}$$

Equation (2-3) serves to relate the end deflection, δ, applied force, F, and induced stress, σ_{max}; given the length, L, width, W, and thickness, t, of the beam and Young's modulus, E, of the material [30]. (Polycrystalline silicon has a Young's modulus of 160 GPa.) By placing realistic limits on what could be fabricated (such as minimum width to allow for definition of piezoresistors and minimum thickness of films to

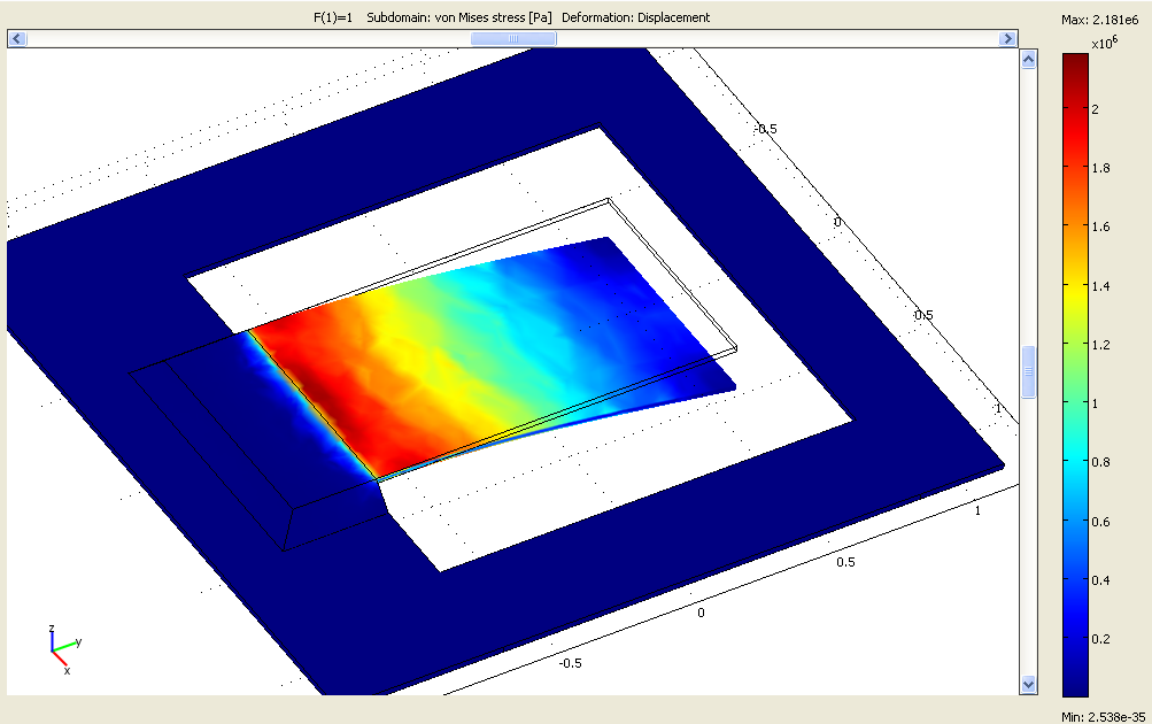


Figure 2-1: COMSOL simulation demonstrating concentration of stress at the fixture point in polysilicon, cantilever-beam structure. (Thin black lines indicate original position. Beam is 130 µm-long, 80 µm-wide, and 2 µm-thick; 8 µm over substrate; 1 µN downward force applied 120 µm from fixture point, in center of beam.)

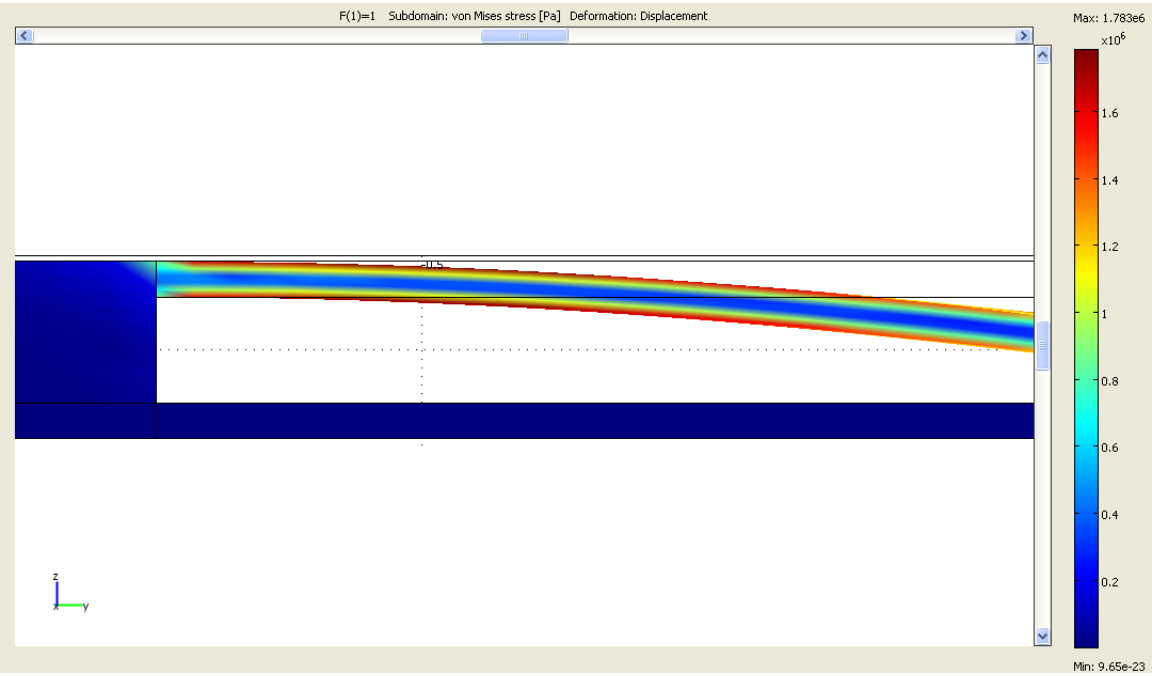


Figure 2-2: Side profile of stress in cantilever beam demonstrating maximum stress at top and bottom surfaces. (Same beam and force as simulated before.)

ensure reasonable uniformity), the following dimensions were found to result in high-stress responses, full range, and realistic dimensions: thickness – 2 μm, width – 80 μm, and length – 120 μm. The range was determined by ensuring that 100 μN would not displace the end of the cantilever more than the 8 μm assumed for the spacing above the balloon. The 8 μm limit was created to ensure that the sacrificial oxide could be deposited and patterned without the layer cracking and peeling off due to internal stresses caused by deposition. With these specifications, the maximum stress associated with a 1 μN force applied to the end of the cantilever is predicted to be 2.25 MPa (COMSOL simulations predict ~2 MPa).

In order to facilitate the presence of a point force at 120 μm from the fixture point, the cantilever was actually designed with a length of 130 μm, giving a 10 μm ledge for the application of the point force. Additionally, in application the sensors would be more likely to encounter a distributed pressure across their surface. Simulations were therefore done to find the maximum stress generated by a generalized force. The point force of 1 μN was divided by the surface area of the cantilever and that pressure was applied to the top surface of the cantilever; this resulted in a maximum stress of roughly half that found with the point force.

2.3 Balloon Actuator

In addition to the sensor, a balloon structure was added for actuation. The balloon is a rather simple actuating mechanism in principle: when the balloon is filled with air pressure its shape deforms to balance out forces. As this occurs

structures attached to the balloon are shifted in place. This can clearly be demonstrated in the microhand where the balloons act as muscles to pull the fist closed (Figure 2-3) [18]. By placing a force sensor in the center of the balloon surface, good contact with the target being gripped can be achieved, allowing for accurate feedback of the gripping force. Balloons could also be designed and mounted in other configurations to permit actuation differing from that demonstrated in Figure 2-3.

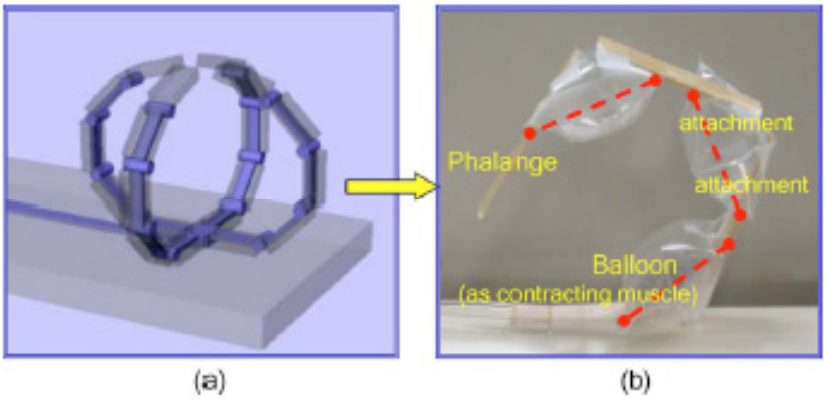


Figure 2-3: (a) Computer drawing of a four-fingered microhand and (b) a macroscale prototype of one finger showing how pneumatic balloons can serve as muscles. Reprinted with permission from [18]. Copyright 2006, American Institute of Physics.

In order to test the sensor structure with and without the balloon, each die contains four of each piezoresistor layout, two on and two off balloon. The two on balloons allow for observation of interference in the force signal, due to stress exerted on the sensing structure by the balloon. Although this interference will undoubtedly complicate sensing of the applied force, it may offer the added benefit of sensing the balloon's inflation/shape. The balloons also demonstrate compatibility with the process used to fabricate the microhand, the sensor's primary application. The two sensors not mounted on balloons allow for simplified testing,

as they are isolated from the effects of a deformable substrate. The balloons were designed to have a surface area of approximately 1 mm by 1 mm, with the sensor placed in the center. This sizing was chosen to give an approximate relative size to the sensor in future applications.

The balloons will be made of Parylene-C which is a unique material because it can be vapor-deposited in a process called vapor deposition polymerization (VDP). In VDP, dimers of Parylene are heated to 150 °C where they vaporize [26]. Further heating to 680 °C leads to dissociation of the two monomers in the dimer. The stable monomers are then pulled into the deposition chamber by vacuum, where contact with the substrate causes polymerization. The monomers have a mean free path of 0.1 cm, allowing them to enter small cavities and form a uniform coating on all surfaces exposed to the vapor. Using this process, Parylene vapor will be 'blown' into a mold cavity (formed in the substrate) where it will polymerize into a balloon.

In addition to its unique deposition process, Parylene-C offers some useful properties. High electrical resistivity allows it to insulate interconnect used to stimulate and sense the sensor response. Water vapor transmission rate is very low; this protects the pneumatic system, allowing it to work in a variety of environments. Similarly, it is impermeable and chemically resistant to most solvents and chemicals. Biocompatibility and biostability have been demonstrated by the manufacturer [26]. It also has good physical adhesion to numerous materials.

2.4 Interconnect

For electrical interconnect aluminum 'wires' will make contact with the piezoresistors, run across the balloon, and terminate in relatively large pads. These large pads serve as bases for wire bonding, which will facilitate connection to a printed circuit board (PCB) that allows macro scale connections to be made using soldering techniques. Pneumatic interconnect will be achieved by forming microchannels in the substrate in the same manner as the formation of the balloon cavities. Essentially, the channels will be long, narrow balloon cavities linking the balloon chambers. The microchannels will be joined together at one point where a large opening will facilitate a macroscale connection. This single point will provide pressure to all of the balloons on die. This limits independent actuation of the balloons, but it is not necessary for testing the sensors and significantly simplifies testing and the design itself.

Finally, as there are four of each sensor design on a die (two on a balloon and two off), the two in each set are arranged in a chain, with the interconnect of the second sensor winding around the first sensor (Figure 2-4). The aluminum interconnect of the second sensor runs over the breadth of the first balloon. This will demonstrate that sensors can be arranged in a linear array without causing damage to the interconnect or signal interference.

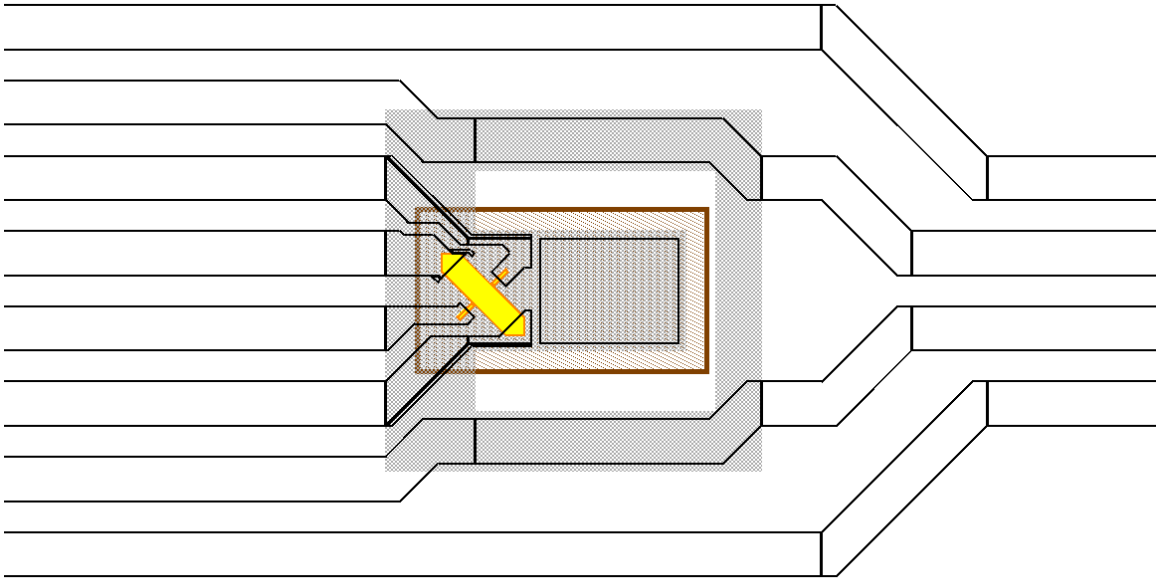


Figure 2-4: L-Edit layout with aluminum interconnect (white with black outline) winding around the first force sensor structure on its way to the second sensor in the array.

2.5 Piezoresistor Layouts

The placement of piezoresistors allows for stress monitoring in different regions of the structure. Additionally, different arrangements allow for direct conversion of stress to a voltage signal using bridge networks. Regardless of design, positioning is critical to monitor the regions of greatest stress.

What has not been discussed thus far are the doping levels and purpose of the dopant. Dopants are the key to leveraging semiconductors: dopants allow them to act as either insulators or conductors. Without any dopants, which are effectively impurities in the semiconductor material, the semiconductor has a very high resistivity. By introducing even a small number of impurities into the silicon lattice, the resistance can be reduced significantly so that it acts as a conductor. This occurs because each atom of an impurity provides either an extra electron (donors) or an

extra hole (acceptors). The dopants therefore provide extra free carriers in the semiconductor and thus provide a path for electrons or holes to flow in an electric current.

By varying the impurity concentration, the resistance of the material can be selected. It is in this fashion that the piezoresistors will be created from polysilicon. Boron was selected as the dopant as it is a P-type dopant, it provides a hole for an electron to occupy in the material, and GF in polysilicon is strongest with P-type doping (Table 2-1).

2.5.1 Basic Design

The simplest sensor design has two resistors formed on the cantilever. The larger of the two resistors (Figure 2-5) is placed on the maximum stress region caused by deflection of the cantilever beam, as predicted by simulation in Figure 2-1. Ideally, the stress from the cantilever will be the only source of stress; however, the balloon is also a major source of stress. Figure 2-6 demonstrates how inflating the balloon with a pressure of 10 PSI can completely obscure the stress induced by a 1 μN force on the cantilever beam (Figure 2-1). The stress caused by the balloon is three orders of magnitude bigger. This causes a significant problem in isolating the stress from forces applied to the beam. In an attempt to achieve this isolation, the right and smaller resistor has been added as a reference. Figure 2-1 indicates that the stress caused by the beam's deflection stops at the edge of the fixture point. Because the small resistor is to the right of this point, it should only experience stress caused by the balloon's deformation.

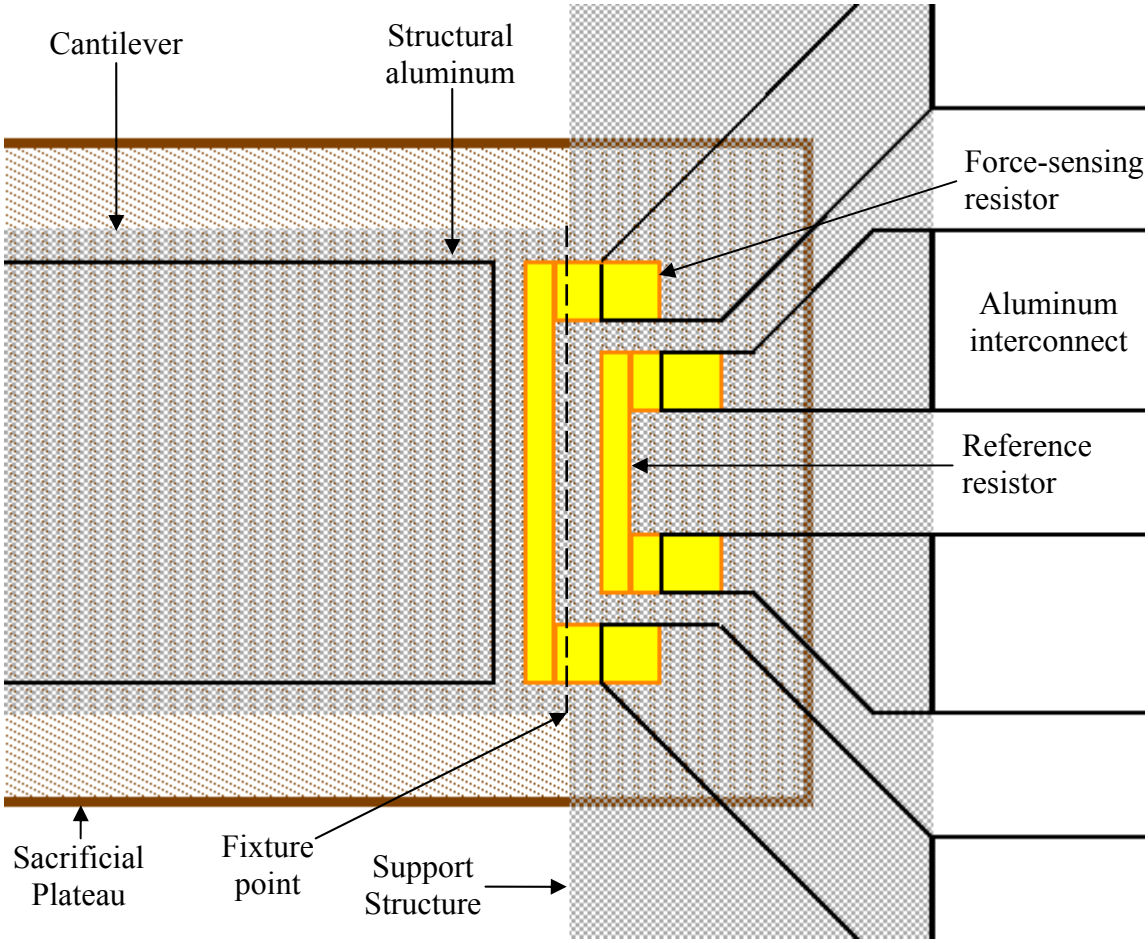


Figure 2-5: Simple piezoresistor sensor design; one on cantilever and one on support structure (yellow with orange outline is resistor, white with black outline is aluminum interconnect, grey is polysilicon support structure and cantilever, and brown is sacrificial plateau).

By applying the following equation (modified from [30]) it is possible to estimate the resistance change that can be achieved from this sensor

$$\frac{\Delta R}{R} = GF\frac{\sigma}{E} = \frac{6\,\beta\,L\,GF}{E\,W\,t^2}F = \frac{3\,\beta\,t\,GF}{2\,L^2}\delta \qquad \textbf{(2-4)}$$

where $\frac{\Delta R}{R}$ is the fractional change in resistivity; GF is the gauge factor of the resistor; σ is the stress induced on the beam; β is an ideality factor; W, L, and t are the dimensions of the beam; E is Young's Modulus for the beam and resistor material; and F and δ are the force applied to and the displacement experienced by the beam,

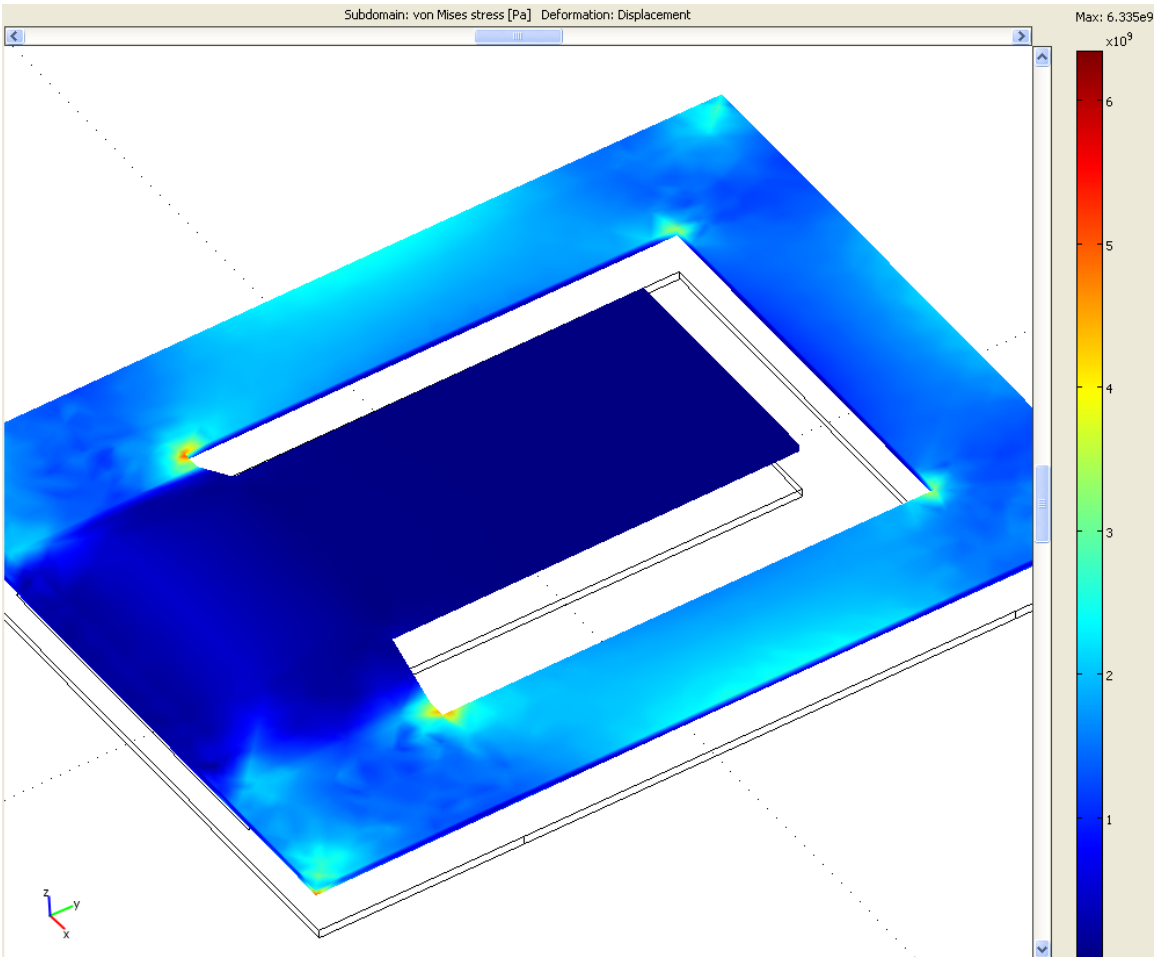


Figure 2-6: Stress induced on the preceding polysilicon structure when balloon is inflated with 10 PSI. The stress completely masks the stress caused by the 1 µN force applied to the cantilever beam. (Entire structure has been elevated above original position, indicated by thin black lines, due to inflation of balloon. Balloon is a 1 mm by 1 mm square, 5 µm-thick, Young's Modulus of 400 kPSI and Poisson's Ratio of 0.33.)

respectively. The ideality factor attempts to account for the fact that the maximum stress induced in the beam will not be experienced by the entire piezoresistor: some regions of the resistor will experience less stress. It ranges from zero to one; accounting for the finite size of the resistors, misalignments of the resistor, non-uniformities in the material, etc. By applying the dimensions chosen in Section 2.2 (80 µm x 120 µm x 2 µm), a gauge factor of -9, an ideality factor of 0.9, and a Young's Modulus of 160 GPa, the equation estimates a change of 0.011% in the

piezoresistor's resistance, for a 1 μN force. COMSOL simulations predict a sensitivity of 0.013%/μN on a 10 kΩ resistor, or 1.3 Ω/μN.

2.5.2 Unsupported Design

In a modification of the basic design, the support plateau has been removed from under the support structure. Figure 2-7 demonstrates that this moves the maximum stress point to around the top of the slope that rises from the support structure to the beam, rather than being on the cantilever at the fixture point (Figure 2-1). This was designed to determine if the plateau support is necessary, because it would be easier to fabricate without the raised support structure (see Section 3.2 Release Considerations, page 44).

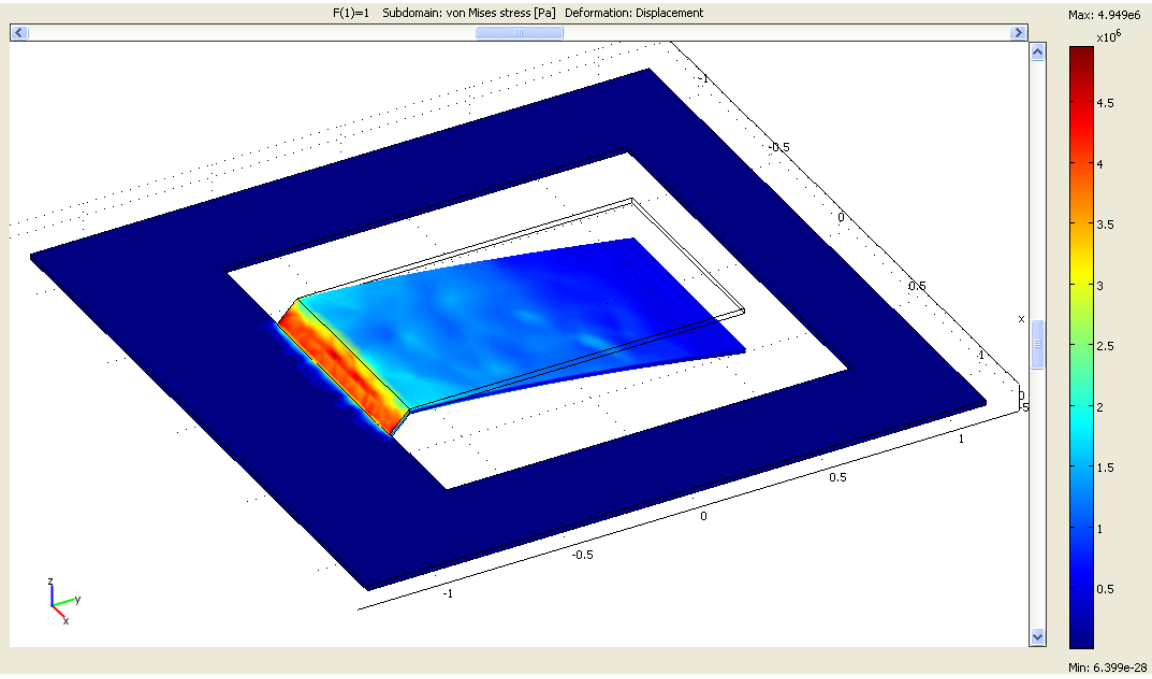


Figure 2-7: Unsupported cantilever design demonstrating the shift in the location of the maximum stress, 1 μN force applied. (Same dimensions and force application as previous simulations.)

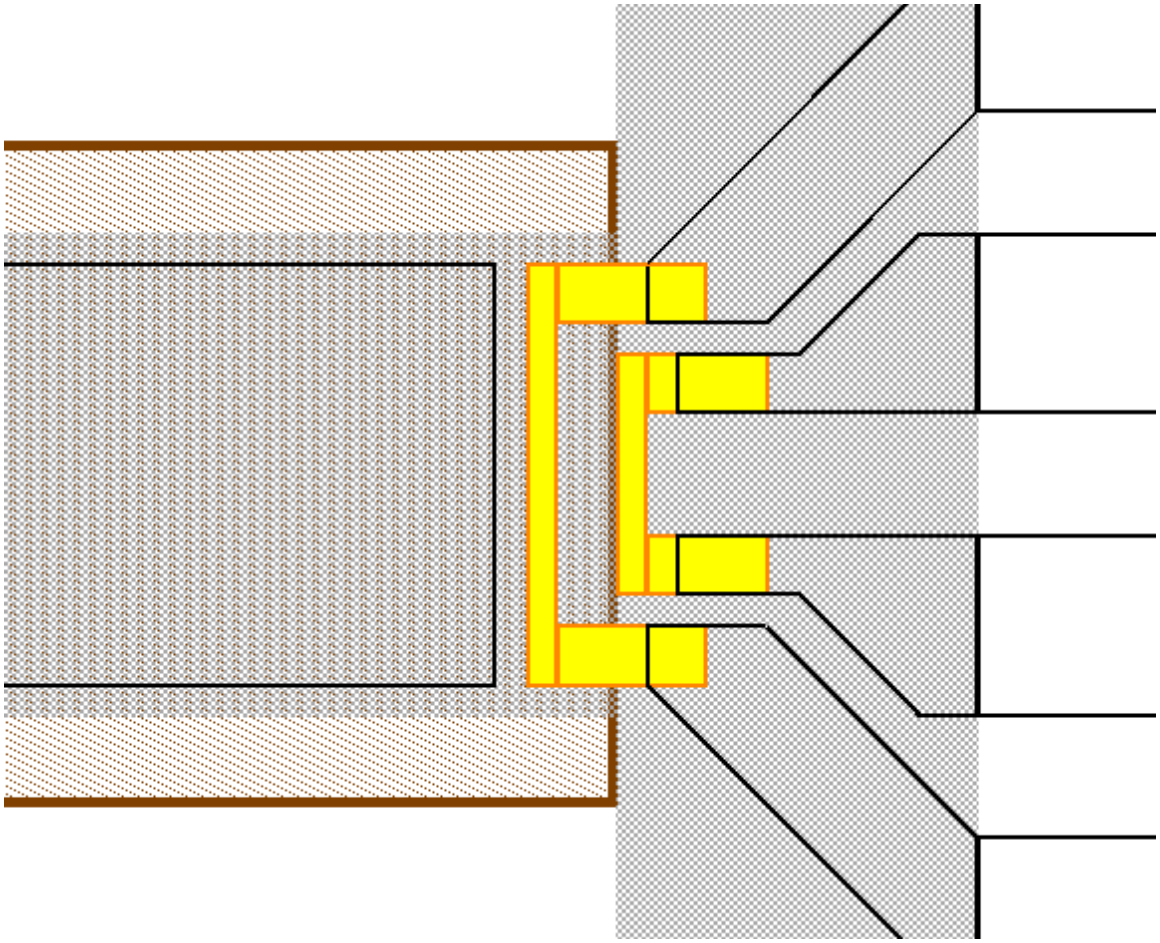


Figure 2-8: Unsupported sensor design with larger resistor at top of cantilever rise and the other at the base of the rise.

Again, there are two piezoresistors; the smaller of the two is placed at the bottom of the cantilever rise and the larger one is at the top of the cantilever rise (Figure 2-8). Notice that the brown, dotted region, the sacrificial plateau, starts at the edge of the cantilever. This is unlike the other designs where the plateau extends into the support structure and creates the raised support structure, ideally concentrating all of the stress at the fixture point in the cantilever. With the plateau starting at the edge of this region, it should take roughly 8 μm, caused by lateral etching, to rise to the cantilever's surface. The spacing in the masks for the

piezoresistors should then place the larger resistor at the top of the rise. COMSOL simulations predict about double the stress (5 MPa versus 2 MPa), but in a different location, and deflection (1.2E-7 m versus 0.7E-7 m) for the unsupported beam design, in comparison to the supported designs, with a 1 μN force applied to each. Sensor sensitivity is predicted at 0.0078%/μN on a 3.5 kΩ resistor, or 0.27 Ω/μN.

2.5.3 Longitudinal Design and Integrated Probe

The next design rotates the piezoresistors 90° to experience longitudinal stress instead of the transverse stress experienced by the previous designs. This will affect the resistance change experienced by the resistors, as stress will be applied along the length of the resistors instead of the width. The previous designs should register a decrease in resistance, whereas these should increase in resistance. The rotation leaves space to run aluminum traces down the edge of the cantilever structure. If the traces are left exposed to the environment (this will not be possible for biological applications, if formed from aluminum, because of aluminum's bioincompatibility), they can serve as electrodes to measure the impedance of the environment; detect signals from objects they are touching, such as nerve fibers; and stimulate the environment with electric energy if the need arises. This design (Figure 2-9) has the resistors put on a slight slant and traversed over the maximum stress region numerous times. The slant gives slightly more space at the opposing ends to allow for misalignments in the lithography process. Multiple, short crossings of the piezoresistors allow for a larger resistance without sacrificing sensitivity. As the maximum stress is concentrated only near the fixture

point and the piezoresistors only respond to stress and strain, resistors extending beyond the maximum stress region are less sensitive to an applied force. Therefore, confining the resistors to the maximum stress region is optimal. The multiple crossings allow the resistance to be increased in order to make its resistance considerably higher than the interconnect, which could serve to add noise, essentially increasing the sensor's signal-to-noise ratio (SNR). COMSOL predicts sensitivity of 0.3%/μN on a 100 kΩ resistor, or 300 Ω/μN.

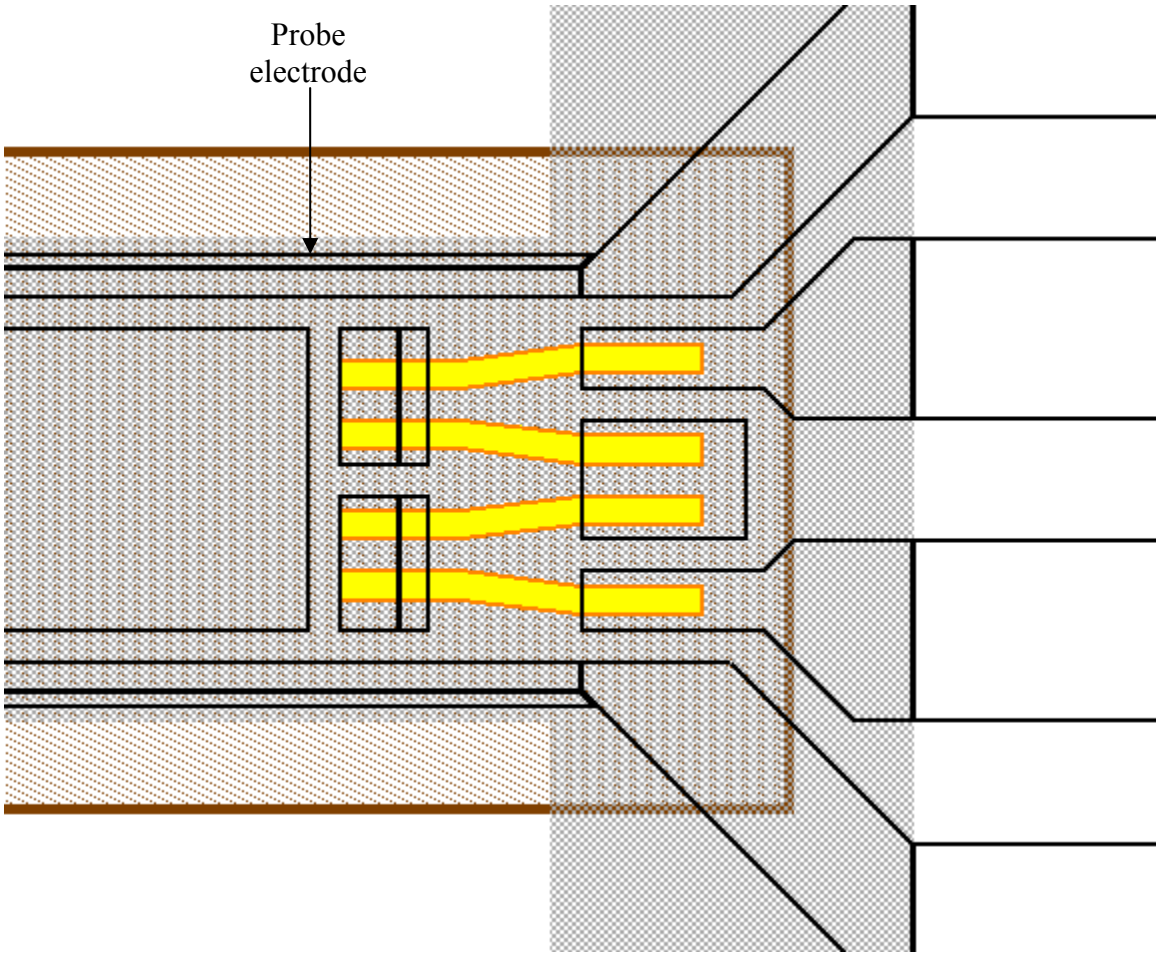


Figure 2-9: Longitudinal sensor design with integrated electrode probe.

2.5.4 Motorola Xducer

Motorola has a rather unique transducer design that they have called the "Xducer[1]." It is similar to the Wheatstone bridge in that it converts a changing resistance to a voltage signal. However, the Xducer does this with one resistor instead of four. The general layout can be seen in Figure 2-10. The large resistor has voltage applied to it at either end creating a current flow down its length. As the resistor is stressed, a current gradient is set up between the two taps that results in a voltage difference between them [27].

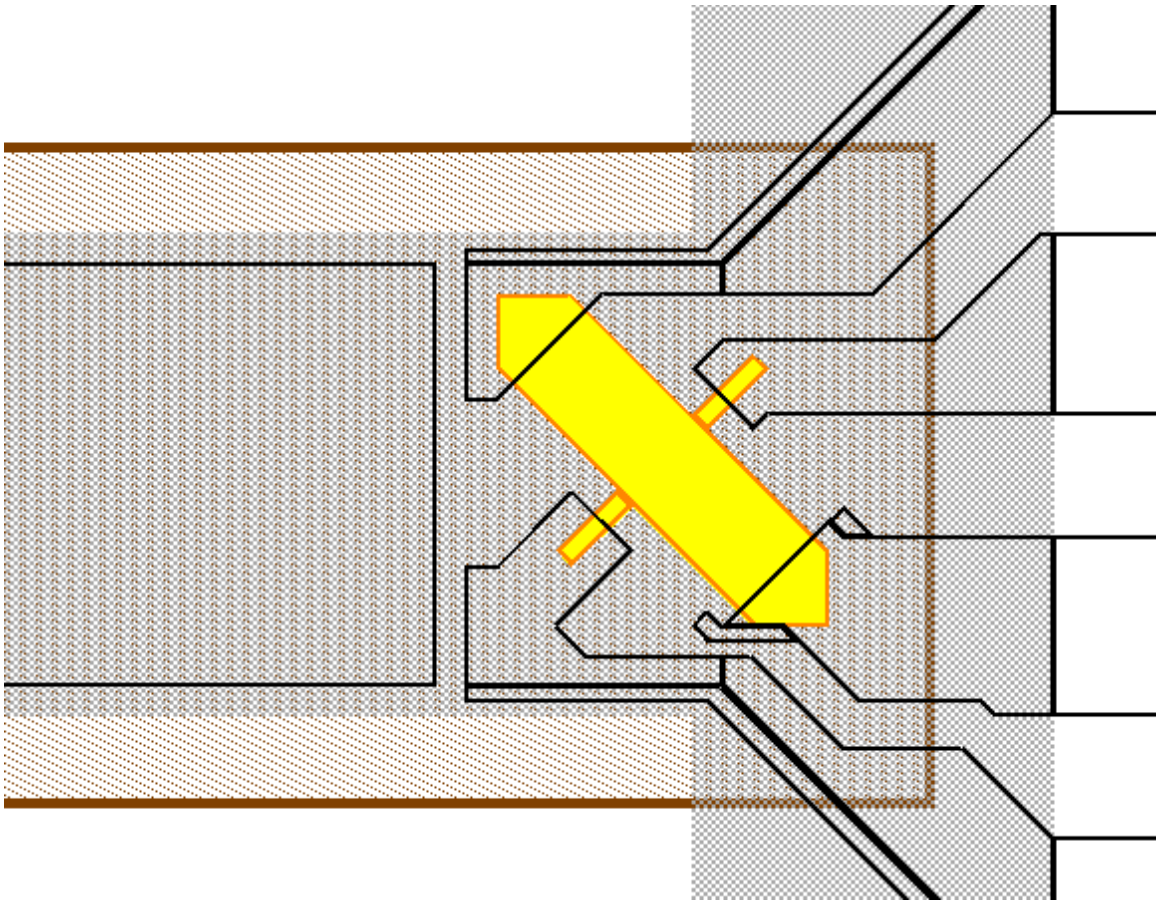


Figure 2-10: Xducer sensor layout; voltage applied to large resistor creates a small voltage difference across the transverse taps when stressed.

[1] Xducer is a registered Trade Mark of Motorola, Inc.

In the original Motorola design the taps come right up to the main resistor. However, they were shifted back in this case to allow for some misalignment. This should not cause any loss of sensitivity, as the taps will not draw any significant current because they will be connected to a high-impedance op-amp or DAC thereby ensuring no voltage drop across the short stub from the resistor to the aluminum interconnect. The largely oversized interconnect junctions for the main resistor are also arranged to allow some misalignment, without affecting the current uniformity. As the stress between the taps is critical, the region between the taps was shifted just to the left of the theoretical fixture point for the cantilever, coincident with the location of maximum stress. COMSOL simulations predict a 75 μV/V/μN sensitivity, or 380 μV/μN with a 5 V supply.

2.5.5 Motorola Picture Frame

Motorola eventually switched its diaphragm-based pressure sensor mechanism from the Xducer to a Wheatstone bridge configuration [27]. Motorola uniquely applied the bridge on only one edge of a square diaphragm, as opposed to the traditional spacing of one of resistor at each edge of the square diaphragm (Figure 2-11 left). The Picture Frame allows for a more compact design than a traditional arrangement with slightly lower response sensitivity. The lower sensitivity is caused by the lower stress experienced because only a portion of the resistors are located at maximum stress locations. However, the Picture Frame does have greater sensitivity than the Xducer. Instead of one resistor changing, all four

resistances change and they vary in opposite directions, as depicted in Figure 2-11 (Right), combining their effects to make a larger output swing.

The implementation used in this project is essentially the same as the Picture Frame because all resistors are located at the fixture point of the cantilever (Figure 2-12). The piezoresistors experience a similar stress profile, with the resistor at the edge getting the maximum effect and the others a degraded magnitude. Regardless of this degraded effect at the other resistors, the combined output change is still greater than that of the Xducer or the single resistor sensors. COMSOL confirms this with a simulated sensitivity of 200 μV/V/μN, or 1 mV/μN with a 5 V supply.

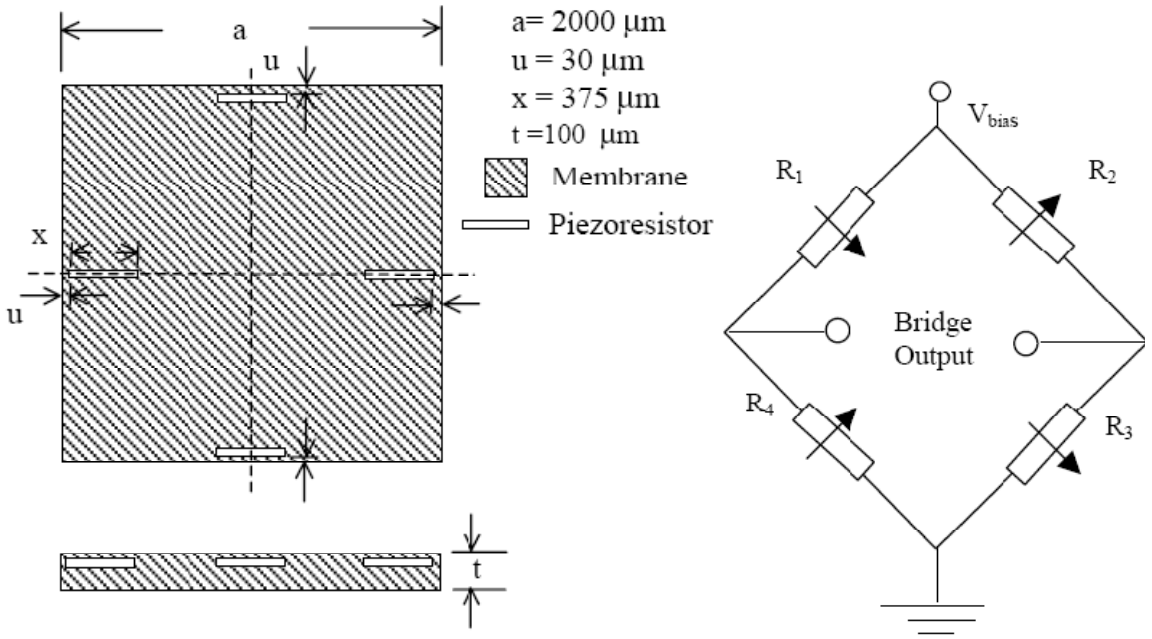


Figure 2-11: Standard Wheatstone bridge piezoresistor layout on diaphragm based pressure sensors (left) and schematic symbol of standard Wheatstone bridge indicating connections and direction of resistance change in resistors caused by pressure (right). Reprinted with permission, [29], © 2002 IEEE.

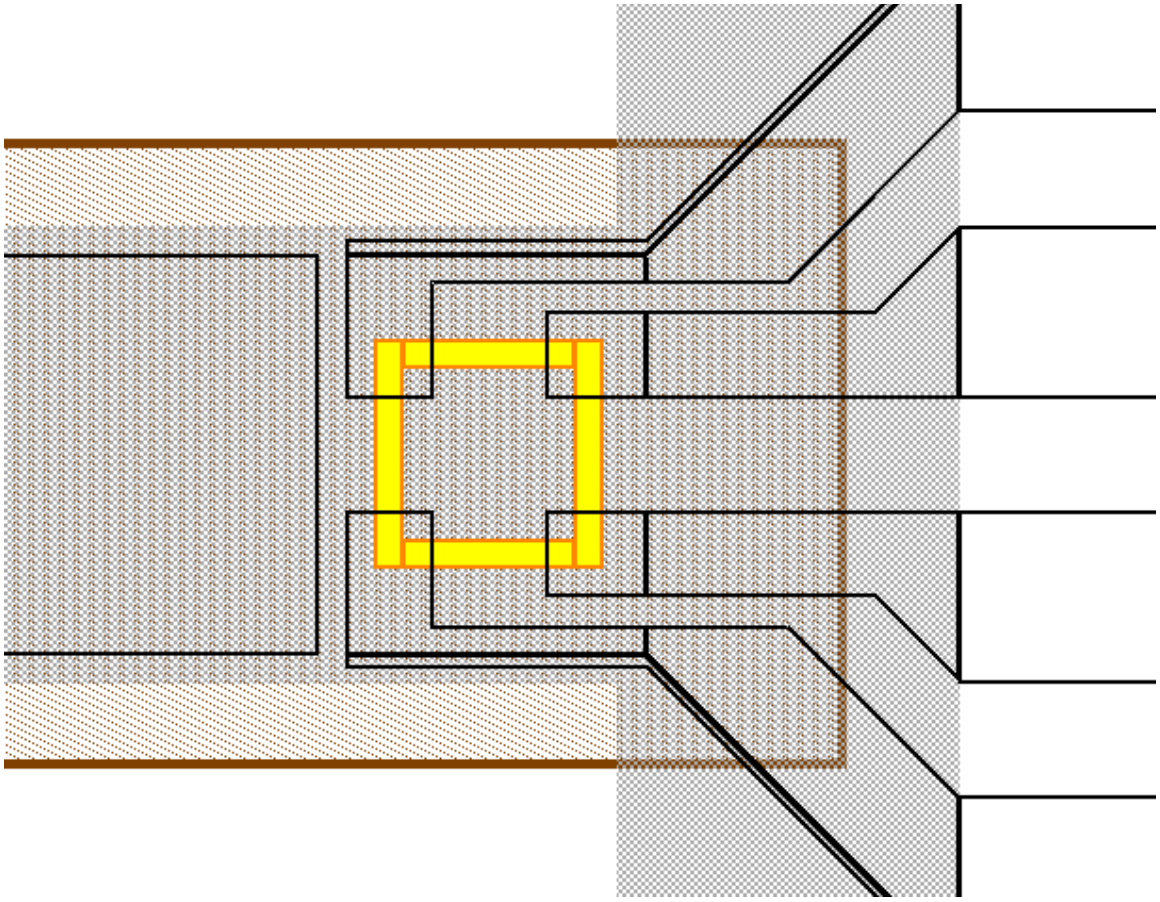


Figure 2-12: Picture Frame transducer: essentially a Wheatstone bridge with only one resistor on the maximum stress point and the remaining resistors experiencing reduced stress.

2.5.6 Advantages of Bridge Circuits

Bridge circuits offer many advantages, particularly when they are implemented on-device. The first and most obvious advantage is their conversion of the resistance variation to a voltage variation that can be easily read by an Analog-to-Digital Converter (ADC). Additionally, because of the balanced construction of the bridge (all resistances being equal) the output of the bridge is centered at zero making its output easier to interpret. Because of these advantages, even the sensor designs not utilizing an on-device bridge may be connected to a bridge circuit before being connected to an ADC. However, they will not receive the additional benefit of

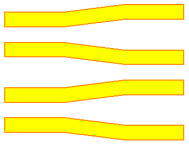
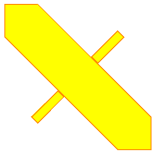
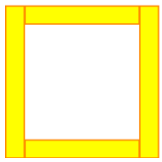
having four piezoresistors acting as a full bridge, such as Motorola's Picture Frame. Nonetheless, if some of the single piezoresistors are set up in a bridge together their effects may be increased. For instance, if sensors on either side of a gripper are connected in a half bridge (two sensors) they should experience the same forces due to the symmetry of the forces exerted by the gripper on the object, and the half bridge will double the output of the overall system.

When the resistors are fabricated in the device/sensor, there is an added compensation advantage. Because all of the resistors experience the same ambient environment, any variation in their resistances is nullified by the bridge's inherent balance. For instance, all resistors vary to some degree based on temperature. Since all the resistors are located in the same area and are of the same material and size they all experience the same change in resistance, nullifying the effects of temperature on the sensor's output. Additionally, the bridge's fabrication as a whole limits the final effects of variation in fabrication results. For example, if the dopant concentration is off slightly due to some processing parameters all of the resistors will experience the same effect. This prevents a need to make changes in the electronics monitoring the sensor's output in order to match the new resistance of the sensor.

2.5.7 Layout Summary

Table 2-2 summarizes the different layouts detailed above.

Table 2-2: Summary of Piezoresistor Layouts

	Basic	Unsupported	Longitudinal	Xducer	Picture Frame
Layout					
Sensitivity	0.013%/μN 1.3 Ω/μN	0.0078%/μN 0.27 Ω/μN	0.3%/μN 300 Ω/μN	75 μV/V/μN 380 μV/μN	200 μV/V/μN 1 mV/μN
Pros	Reference resistor	Simpler fabrication	High sensitivity Integrated probe	Voltage output and bridge compensation	Highest sensitivity and bridge compensation
Cons	Low sensitivity	Lowest range and sensitivity	No stress reference	No stress reference	No stress reference

2.6 Sensor Variations

In addition to the variations already mentioned two other characteristics were varied in the designs to observe their effects on sensitivity. First, aluminum was deposited on portions of the cantilever not already in use by the piezoresistors or the aluminum interconnects. This structural aluminum (Figure 2-5) serves to thicken the beam, increasing rigidity and concentrating stress at the piezoresistors. This was done in half of the dice on each wafer. All of the sensors in the Piezoresistor Layouts Section (2.5) demonstrate additional aluminum blocks on the cantilever beams. Second, the length of some cantilevers was tripled. This should triple stress (σ_{max}), and therefore triple force sensitivity, but at a cost of 95% of the sensing range. This trade-off occurs because the additional length creates more stress for a smaller applied force (F) but the beam's floating end will contact the balloon sooner as it is easier to deflect (δ) the longer beam, Equation (2-3).

3 Fabrication

3.1 Process Overview

Processing begins with 100 mm, mechanical grade silicon wafers. Mechanical grade wafers are acceptable, as none of the electrical properties of the substrate will be used. A 0.5 μm thick layer of silicon dioxide (oxide) is thermally grown on the wafers. This will later serve as the top of the mold cavity for the balloon. On top of this a 1500 Å layer of silicon nitride is deposited by low pressure chemical vapor deposition (LPCVD). Then a tetraethylorthosilicate (TEOS) process is used to form an 8 μm silicon dioxide layer. This will serve to support the cantilever as a sacrificial layer.

The first lithography step defines the sacrificial plateaus, using the sacrificial mask (Figure 3-2 (b)). A combination of reactive ion etching (RIE) and buffered oxide etch (BOE) will be used to etch the TEOS and stop on the underlying nitride layer, protecting the mold's thermal oxide. A cross-sectional view after the completion of the foregoing steps is depicted in Figure 3-1 (a).

Next, the structural polysilicon layer will be deposited to the aforementioned 2 μm thickness. The polysilicon layer will be patterned to form the cantilever and its support structure. The top of this layer is oxidized to form a very thin (100 Å) oxide that will be used as a stress buffer for the next layer: nitride. This oxidation is done thermally and serves to anneal the polysilicon so that it will be straight when released from the sacrificial layer. The 1000 Å silicon nitride layer is deposited in LPCVD. The piezoresistive layer is formed using LPCVD to deposit 1000 Å of

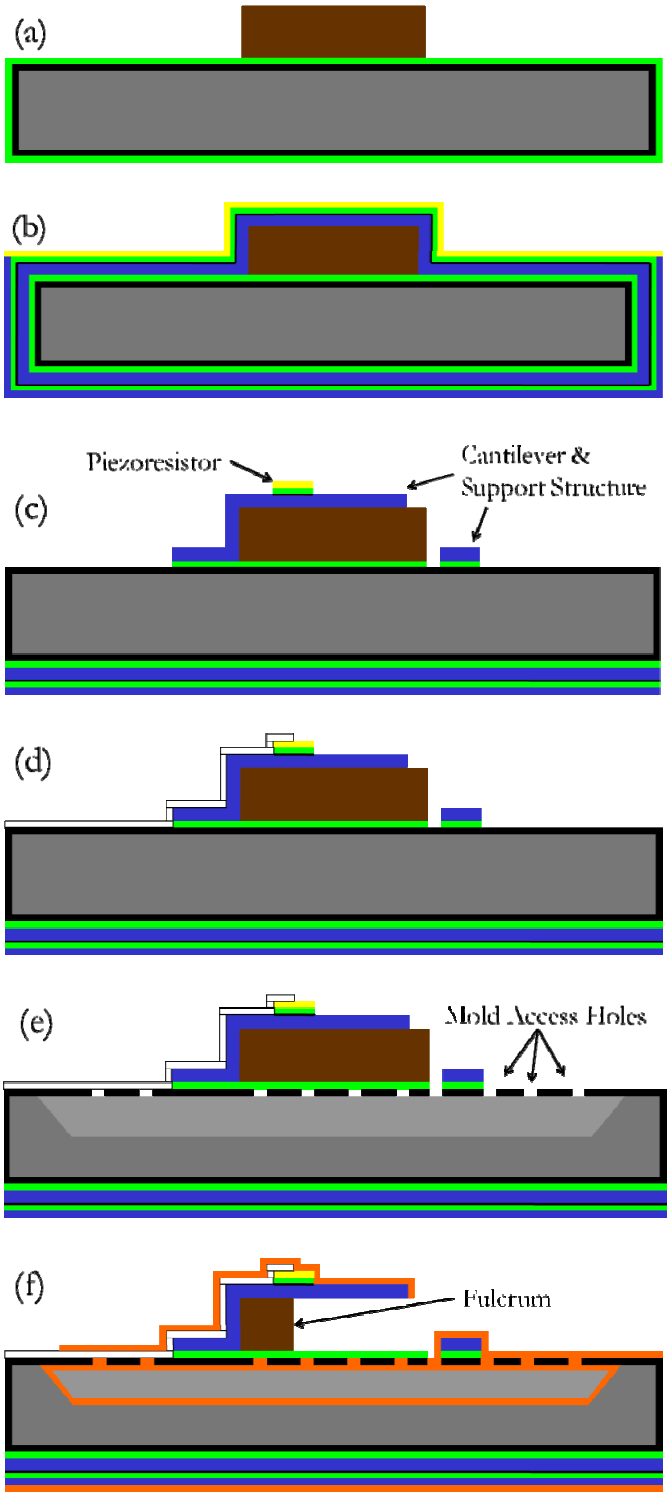


Figure 3-1: Fabrication begins with an oxide/nitride stack and a sacrificial plateau patterned in 8 µm-thick TEOS (a). 2 µm polysilicon, thin oxide, thin nitride, and thin, boron-doped polysilicon layers complete the film stack (b). RIE defines the piezoresistors in the thin, doped polysilicon and the cantilever structure in the 2 µm polysilicon (c). Sputtered aluminum is patterned to form electrical interconnect (d). RIE defines access holes in the underlying oxide and exposes the silicon substrate to be etched by XeF_2 to form the mold cavity (e). Parylene forms the balloon membrane and seals the access holes. Access windows to the aluminum interconnect and sacrificial plateau are ashed in the Parylene. BOE accomplishes a partial etch of the sacrificial plateau to release the cantilever and leave a fulcrum for stress localization (f). Note: Not to scale.

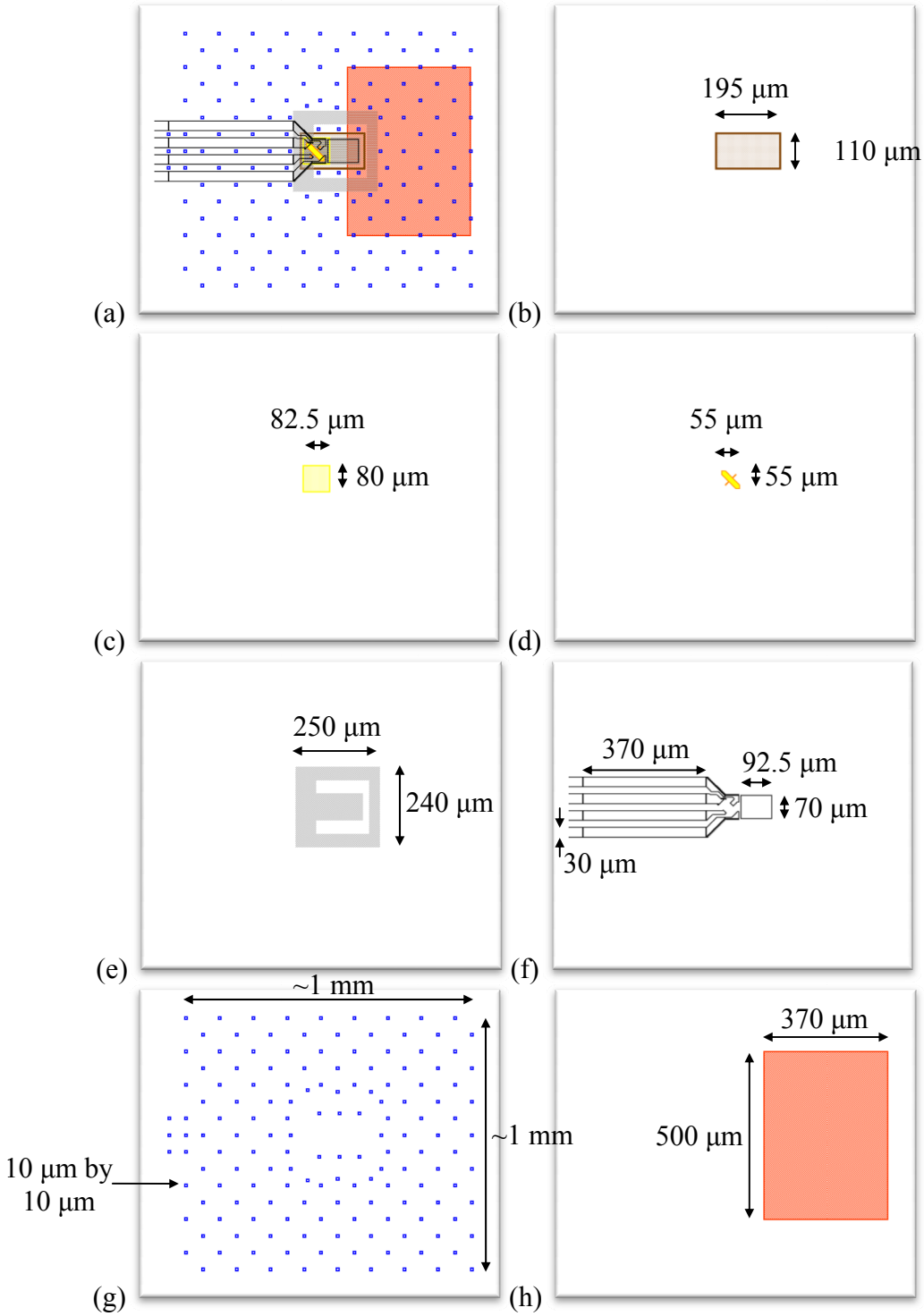


Figure 3-2: L-Edit mask files shown overlaid (a) and individually, in order of use – sacrificial (b), piezoresistor1 (c), piezoresistor2 (d), polysilicon (e), aluminum (f), mold (g), and release (h) (scale and relative position within frame is maintained).

polysilicon and is diffusion doped with Borofilm 100. The underlying nitride layer prevents diffusion into the structural polysilicon layer so that it remains highly resistive and keeps the piezoresistors as thin as possible for higher sensitivity. The high resistivity prevents the interconnect from shorting through the structural layer. With the Borofilm removed in BOE, the result of the processing thus far is depicted in Figure 3-1 (b).

The second lithography step and subsequent RIE define the piezoresistors, using a double mask process (Figure 3-2 (c & d)). A thick photoresist, AZ9260 from AZ Electronic Materials, was used for better topology coverage and thickness control. AZ9260 allows for coatings of 12 μm in one spin and feature definition on top the 8 μm topology of the sacrificial plateaus. The polysilicon support structure and cantilever are defined with the third mask (Figure 3-2 (e)) and an additional RIE (Figure 3-1 (c)).

Aluminum is then sputtered onto the surface of the wafer and patterned with the fourth mask (Figure 3-2 (f)) and aluminum etch (Figure 3-1 (d)). The wafers are sintered to improve the bond between the aluminum and the silicon.

Definition of the balloons is based upon the microhand fabrication process [18]. Lithography and RIE define a grid pattern (Figure 3-2 (g)) over the locations of the balloons and pneumatic microchannels, penetrating the thermal oxide and into the silicon substrate. Xenon-difluoride, XeF_2, etches at least 75 μm isotropically into the bulk silicon defining the mold cavity (Figure 3-1 (e)). A coating of Parylene-C, by vapor deposition polymerization (VDP), will create the

balloon membrane on all surfaces of the device and seal the 10 μm by 10 μm access holes used to define the mold cavity.

The final lithographic patterning and ashing in an O_2 plasma, exposes the supporting sacrificial layer near the tips of the cantilever beams and the aluminum interconnect pads using the release layer mask (Figure 3-2 (h)). This facilitates contact with the aluminum interconnect and release of the cantilever. A BOE etch will release the cantilever and leave a fulcrum for stress localizations with the remaining sacrificial TEOS layer. Once this is accomplished, the devices can be packaged for testing and should appear similar to Figure 3-1 (g).

3.2 Release Considerations

Because the lithography will expose only the tip of the cantilever, the BOE will have to etch a significant distance under the cantilever and the PR mask. This should make it possible to control the underetch of the cantilever and leave a portion of the sacrificial oxide flat and intact to act as a fulcrum. However, the accuracy of the etch stop is critical for alignment of the fulcrum and the piezoresistors. The etch progress can be visually observed at various times throughout the etch time to determine the appropriate endpoint. To aid in this determination a release test structure was designed. As shown in Figure 3-3, a mock up of two polysilicon cantilevers, back-to-back, is built on top of a sacrificial plateau. The distance between the edge of the release mask (red) and the center of the structure is the same as the distance to the desired point of the fulcrum point for

the force sensors. The windows in the polysilicon should allow the etching of the TEOS to be monitored and when it is no longer visible the etch will be complete.

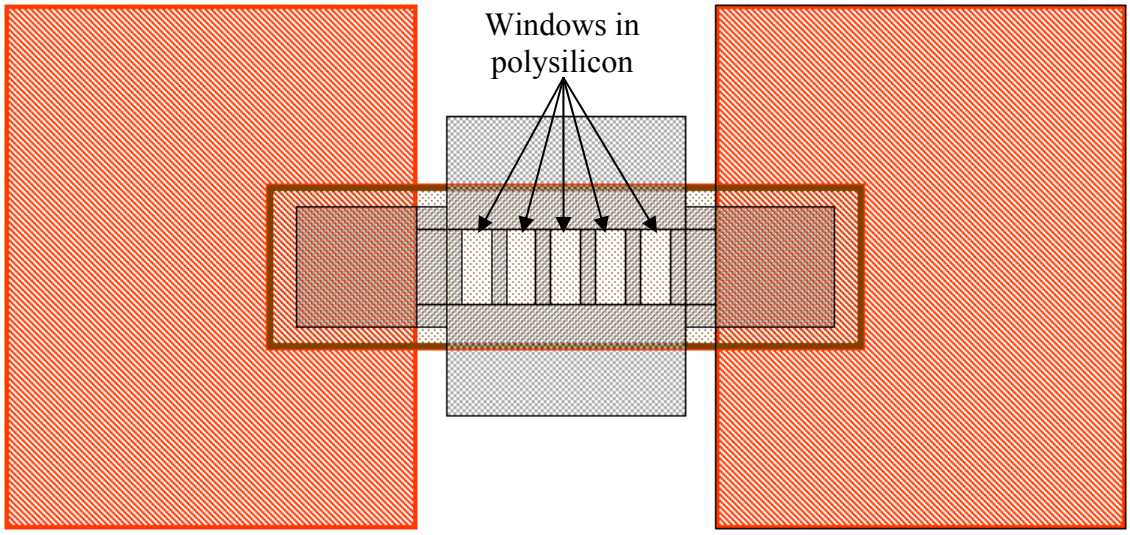


Figure 3-3: Release test structure, polysilicon imitates two back-to-back cantilevers and the middle windows show when the BOE has etched away all of the desired TEOS under the cantilever structures. BOE will have access to the sacrificial TEOS through the red, hashed regions on each end.

3.3 Alignment Considerations

Due to the large lateral etching of the sacrificial layer, it is difficult to consistently and accurately align to this level. To account for this a set of triple alignment marks was created, with a variation of 0, 5, and 10 μm overlap between the crosshair and the encompassing marks (Figure 3-4). Consequently, any amount of overetching would still allow for reasonably good alignment of the layer. The significant overetching also required substantial marks to ensure they were not etched away completely. 50 μm-wide crosshairs were chosen for this purpose. Subsequent layers have more modest widths of 10 μm, allowing them to be captured

by the field of view of alignment microscopes and provide more precise alignment (Figure 3-4).

The alignment of the first layer is a visual attempt to center the final design in the center of the wafer and orient it so the major flat of the wafer is at the bottom of the mask design. The second level, the piezoresistor, is aligned to the sacrificial level. Alignment marks for the third level, polysilicon, are created on both the first and second level (Figure 3-4). This was done because it would be advantageous for both alignment accuracy and precision if all levels could be aligned to the piezoresistor level, but it was unclear if the piezoresistor alignment marks would be useable. The concern of usability arose from possible problems in their definition during etch steps or from seeing their limited thickness through the bulk of the PR. All levels above the polysilicon level were given the option of aligning to the piezoresistor or polysilicon levels.

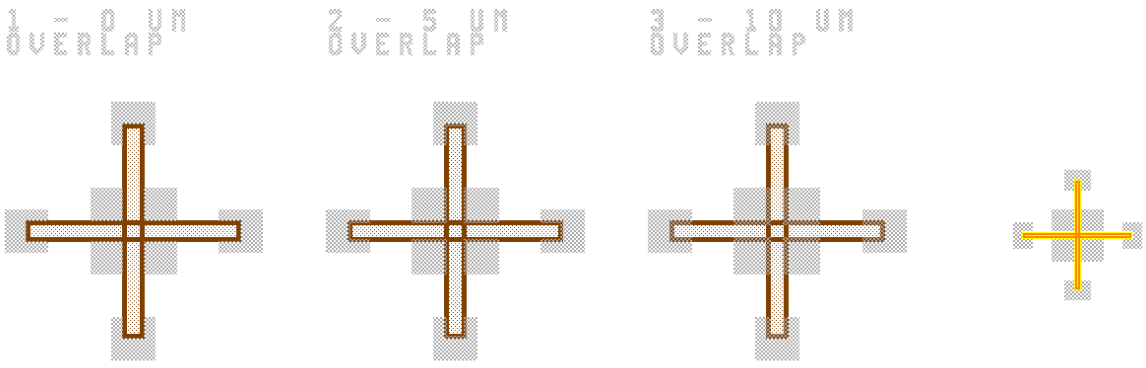


Figure 3-4: Alignment marks between sacrificial (brown) and polysilicon (grey) levels showing the 3 different overlap sets. Additionally, the smaller alignment mark used in later levels, and given as an option for the polysilicon level (yellow with orange outline), is shown on the right allowing for more precise alignment to the piezoresistor level.

3.4 Photoresist experimentation

3.4.1 Coating

AZ9260 from AZ Electronics was used as the photoresist for most steps as it offered film thicknesses up to 12 μm in a single spin. The following recipe was designed to achieve a coating thickness of roughly 12 μm [31]:

Table 3-1: AZ9260 Spin Coat Recipe

Parameter:	Value:
Velocity 1	500 RPM
Ramp 1	500 RPM/s
Time 1	15 s
Velocity 2	1500 RPM
Ramp 2	500 RPM/s
Time 2	30 s
Velocity 3	END

Coating begins with a few drops of MicroPrime P-20 (adhesion promoter) dropped onto the center of the substrate with a pipette; this is spun onto the wafer with the spin recipe above. AZ9260 is poured on to the center of the wafer to form a puddle with a diameter of roughly 1 inch. Pouring is important as it introduces fewer bubbles than pipetting, which lead to point defects in the photoresist coating. In order to conserve PR this small amount is spread over the substrate by manually tilting and rotating it, allowing gravity to pull the PR out to the edge of the wafer. After spinning the PR with the recipe above, it is soft baked at 110 °C for 3 minutes, directly on a hotplate. Variation in film thickness, indicated by wavy patterns, is normal and does not appear to negatively affect lithography results.

3.4.2 Exposure

Exposures were accomplished with a broadband light source using a contact aligner. A dose of roughly 1440 mJ/cm^2 was used except where noted. Hard and vacuum contact methods were used with no notable difference in results.

3.4.3 Development

Microposit MF CD-26 by Shipley, a TMAH-based developer, was used to develop the photoresist. The development of the photoresist was primarily done by soaking the wafer in a container of CD-26. The conclusion of development was observed by waiting for the exposed PR (which turns cloudy during development) to clear in the exposed regions. This generally took about 7 minutes depending on the freshness of the developer. Slight agitation was added by tilting the dish from side to side. Visual endpoint detection was used when the majority of the level was exposed, but when only small features were exposed it became necessary to stop periodically and inspect the wafer with a microscope. Once developed the wafers were rinsed on both sides under a moderate stream of running deionized water (DI) and then blown dry with an air gun.

Post-development or hard-bakes were not generally performed, except when attempting to increase feature size or longer RIE etches were to be performed. With this process, lines of 8 μm were resolved as 4.5 μm, 6 μm lines as 2.5 μm, and 3 μm lines were still present, although undersized as shown in the resolution test pattern in Figure 3-5.

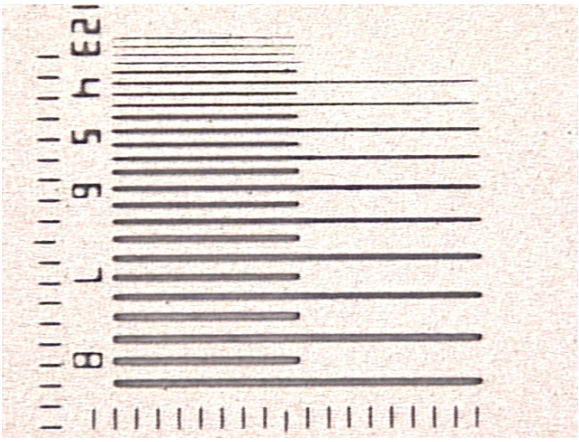


Figure 3-5: Example of resolution test pattern generally achieved with lithography process used in this project (20x).

3.5 Initial Film Depositions

The following process was used to clean the wafers and is based on the process designed by RCA:

1) 10 minutes in SC1 (APM) at 75 °C that consists of 4.5 L of de-ionized water, 300 mL ammonium hydroxide, and 900 mL of hydrogen peroxide. (Removes organics, metals, and particles.)
2) 5 minute cascade rinse in DI water.
3) 1 minute dip in 1:50, HF:H_2O. (Strips native oxide.)
4) 5 minute cascade rinse in DI water.
5) 10 minutes in SC2 (HPM) at 75 °C that consists of 4.5 L of DI water, 300 mL of hydrochloric acid, and 900 mL of hydrogen peroxide. (Removes alkali ions and metals.)
6) 5 minute cascade rinse in DI water.
7) Spin, rinse, and dry (SRD).

With the wafers cleaned of any contaminants, the recipe in Table 3-2 was used to thermally grow a wet oxide of roughly 5000 Å in a Bruce Furnace. The 1500 Å nitride layer was deposited in a modified Advanced Semiconductor Materials (ASM) LPCVD system (Table 3-3). Plasma-enhanced chemical vapor deposition (PECVD) was tested as a means of depositing the nitride layer faster. This proved ineffective, as the PECVD nitride did not hold up in the BOE (Figure 3-6).

Table 3-2: 1500 Å Wet Oxide Recipe for Bruce Furnace

Step:		Time: (min)	Temp: (°C)	Gas Flow: (lpm)
1)	Boat Out –		25	5 N_2
2)	Start –	1 s	800	10 N_2
3)	Push In –	12	800	10 N_2
4)	Stabilize –	20	800	10 N_2
5)	Ramp Up –	20	1000	5 N_2
6)	Stabilize –	10	1000	5 N_2
7)	O_2 Flood –	5	1000	10 O_2
8)	Soak –	37	1000	2 O_2 & 3.6 H_2
9)	N_2 Purge –	5	25	15 N_2
10)	Ramp Down –	35	25	10 N_2

Note: Gas flow rates on Bruce Furnace are in liters per minute.

Table 3-3: 5000 Å Factory Nitride Recipe for ASM LPCVD

Step:		Time: (min)	Temp: (°C)	Pressure: (mTorr)	Gas Flow: (sccm)
1)	Reset –		380		
2)	Status 1 –	10 s	380		
3)	Slow Pump –	15	810	0	
4)	Pump Down 1 –	6	810	0	
5)	Leak Check –	1	810	< 250	
6)	Ramp Up 1 –	40 s	810	300	150 N_2
7)	Heat Up –	20	810	300	150 N_2
8)	Ramp Down 1 –	1	810	1	1 N_2
9)	Pump Down 2 –	2	810	0	
10)	Ramp Up 2 –	40 s	810	400	120 SiH_2Cl_2 & 38 NH_3
11)	Nitride –	~23	810	400	120 SiH_2Cl_2 & 38 NH_3
12)	Ramp Down 2 –	40 s	380	1	1 SiH_2Cl_2 & 1 NH_3
13)	Pump Down 3 –	1	380	0	
14)	N_2 Pump 1 –	15 s	380		20 N_2
15)	Ramp Up 3 –	40 s	380		100 N_2
16)	Post Purge –	10	380		100 N_2
17)	Pump Down 4 –	1	380	0	
18)	Isolate –	15 s	380		
19)	N_2 Pump 2 –	15 s	380		
20)	Backfill –	10	380		
21)	End –	1 s	380		

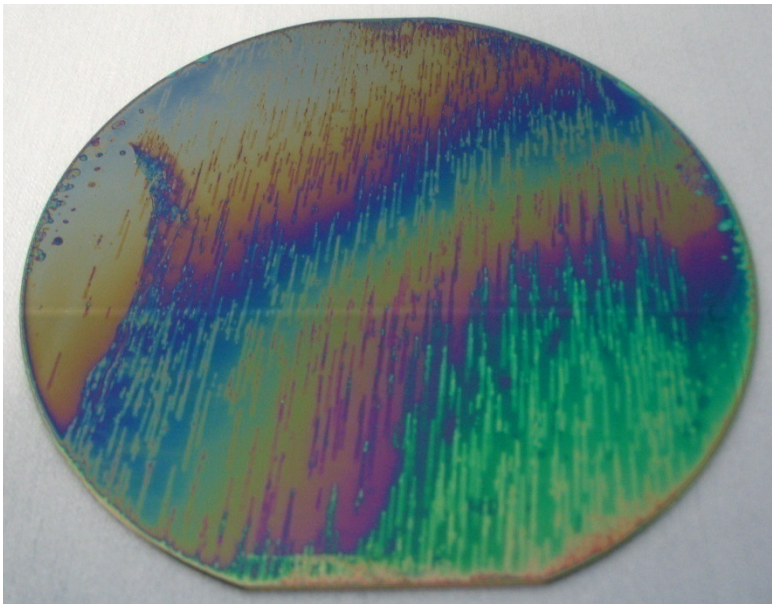


Figure 3-6: Damaged PECVD nitride after a 10 minute exposure to 5.2:1 BOE. Green on bottom right of wafer was original color before BOE exposure.

The 8 μm TEOS was deposited in 1 μm layers by repeating the low-stress recipe 8 times (Table 3-4). The 1 μm layers allowed for cleaning of the chamber between depositions to ensure that buildup in the chamber did not damage the machine (Applied Materials P5000) or alter the process conditions. The low stress properties of the TEOS recipe are very important to ensure that the substantially thick TEOS layer does not begin to flake off before it can be patterned due to internal stress between the film layers. It should be noted that the P5000 is set up to run 150 mm wafers. It was therefore necessary to carry the 100 mm device wafers on 150 mm carriers. The carrier wafers have a 150 mm-diameter, ~250 μm-deep recess in the center to keep the 100 mm wafer from sliding out.

Table 3-4: 1 µm Low-Stress TEOS Deposition for Applied Materials P5000 PECVD

Step:		Time: (s)	Temp: (°C)	Pressure: (Torr)	Gas Flow: (sccm)	RF Power: (W)	Electrode Gap: (mils)
1)	Setup –	15	390	9	285 O_2 & 400 TEOS	0	220
2)	Deposit –	87	390	9	285 O_2 & 400 TEOS	290	220
3)	Descum –	15	390	0	285 O_2	50	999
4)	Low Clean –	45	0	0	400 O_2 & 300 C_2F_6-B	650	999
5)	Stabilize 1 –	15	0	> 5	600 O_2 & 500 C_2F_6-B	0	180
6)	High Clean –	25	0	10	600 O_2 & 500 C_2F_6-B	650	180
7)	Pump 1 –	15	390	0		0	180
8)	Stabilize 2 –	15	390	> 5	285 O_2 & 400 TEOS	0	180
9)	Season –	10	390	9	285 O_2 & 400 TEOS	350	180
10)	Pump 2 –	15	400	0		0	999

Note: Wafer is out of chamber during clean and season steps (4-10).

3.6 Sacrificial Plateau Definition

To withstand the long etch times in the RIE process, a hard mask was formed out of 0.5 µm aluminum. A CVC 601 sputtering tool was used to perform the deposition. An 8 inch Al/Si (1%) target was used with 2000 W of continuous RF power. The target was pre-sputtered for 5 minutes and then the deposition was run for 24 minutes, at a pressure of 5 mTorr with 20 sccm of argon flowing.

A standard wafer coat and develop track (SVG 88 Series) using Fujifilm HPR-504 photoresist was used to coat and develop the wafer with a 1.25 µm-thick PR. An exposure time dose of roughly 120 mJ/cm^2 was used. The pattern was transferred to the aluminum with an aluminum etch bath (16 H_3PO_4 : 1 HNO_3 : 1 CH_3COOH : 2 H_2O) at 40 °C; completion of the etch was done visually. Careful

examination of the completion of the aluminum etch is important to ensure accurate feature definition as demonstrated in Figure 3-7, where the aluminum etch was incomplete. After the aluminum etch, the PR was stripped in a 10 minute solvent strip (5 minutes in two different solvent baths, a 5 minute rinse, and an SRD process) using PRS-2000 from Baker.

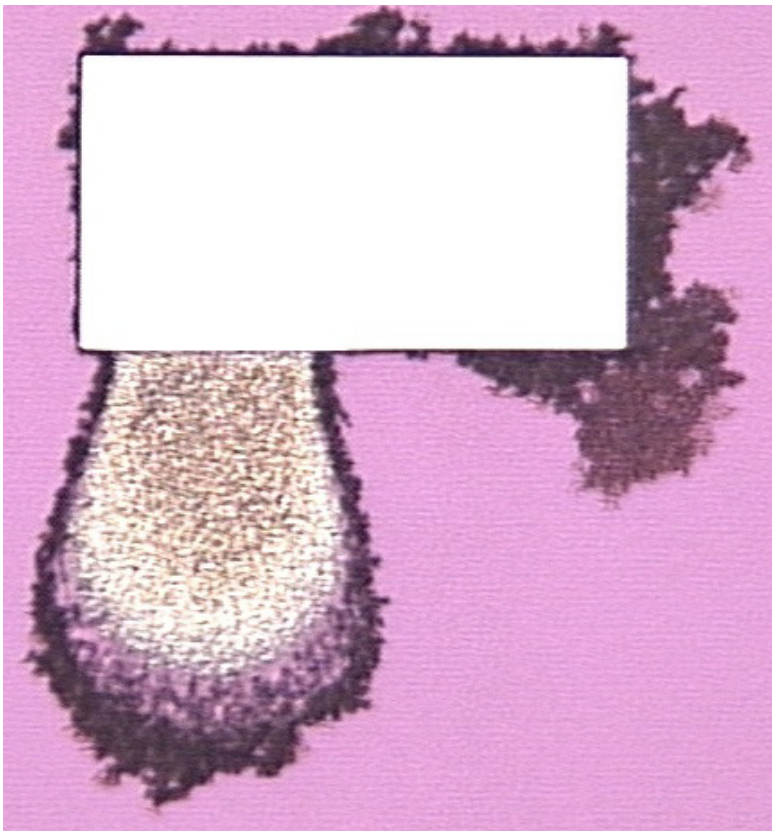


Figure 3-7: Bottom left, bright bulge indicates an incomplete aluminum etch, resulting in a deformed feature. Black coral-like growth around aluminum feature is result of pitting caused by polymer formation around the feature during RIE etching.

With the pattern established each wafer was etched in an RIE oxide etch recipe for 100 minutes. Because continuous etching led to overheating the wafers and the formation of a polymer that interfered/stopped etching (Figure 3-7), the etch was completed in 5 minute increments with at least 15 minute cool-down

periods between etches. Periodic ashes were also implemented to remove the polymer when it was observed. The dry etch was completed in a Drytek Quad unit. The chamber was cleaned with a 5 minute O_2 clean as follows: 100 sccm O_2, 300 mTorr chamber pressure, and 280 W of RF power to generate the plasma. Following the clean, the oxide etch recipe was executed for 5 minutes per carrier in order to season the chamber and the carrier wafer for the process. The oxide recipe used involves 50 sccm SF_6, 50 sccm CHF_3, 140 mTorr, and 200 W. This achieved an etch rate of roughly 600 Å per minute. With the dry etch completed so that roughly 6 μm of TEOS was removed, the remaining TEOS was removed with a 10 minute submersion in 5.2:1 BOE (Ammonium Fluoride : Hydrofluoric Acid). After inspection the aluminum was stripped in the aforementioned aluminum strip, rinsed for 5 minutes, and SRD. (Note: RF power in Drytek Quad has questionable accuracy and chamber 1, used for these etches, commonly reports a stronger output than specified in the recipe.)

Plateau definition with BOE alone was attempted, but neither aluminum nor photoresist can adhere to the TEOS throughout the 8 μm etch. As a result, the features are deformed as depicted in Figure 3-8.

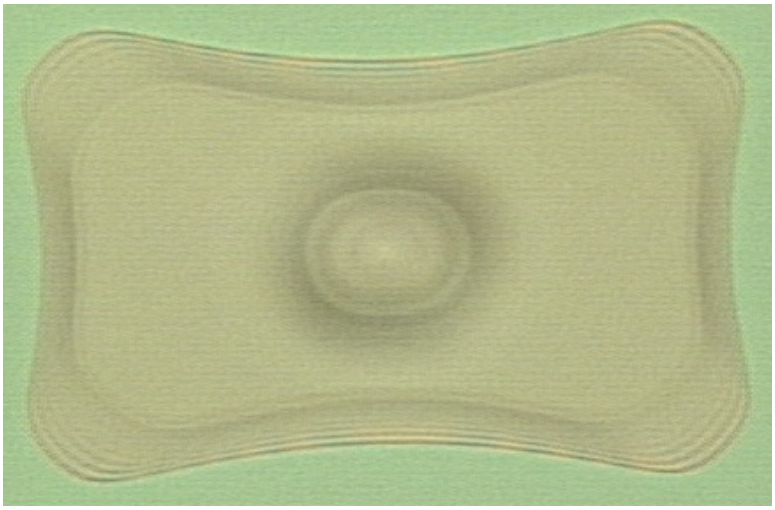


Figure 3-8: Typical sacrificial plateau achieved through wet etching alone. Delamination of the mask resulted in bowing of the rectangular features, increased lateral etch rate, and uneven plateau height (The central circle is raised above the plateau and has a summit of the ~6 µm).

3.7 Thin Film Depositions

Once the sacrificial plateaus were defined, a 10 minute SC2 clean, 5 minute rinse, and SRD prepared the wafers for film depositions. The structural polysilicon layer, insulation layers, and piezoresistor polysilicon layer were deposited to form the sensor film stack. The 2 µm, structural polysilicon deposition was done using the ASM LPCVD system and the recipe in Table 3-5. The top of the structural polysilicon layer was oxidized to form a 100 Å dry oxide in a Bruce Furnace (Table 3-6). Then the 1000 Å nitride and 1000 Å piezoresistive polysilicon layers were deposited in the ASM LPCVD system according to Table 3-7 and Table 3-8, respectively. The silicon nitride serves as a diffusion barrier to the piezoresistor doping, ensuring that the 2 µm polysilicon layer does not short out the aluminum interconnect. The layers on top of the structural polysilicon layer are thin in order

to maximize sensitivity by keeping the piezoresistors in the maximum stress region at the surface of the cantilever (Figure 2-2).

Table 3-5: 2 µm MEMS Polysilicon Recipe for ASM LPCVD

Step:		Time: (min)	Temp: (°C)	Pressure: (mTorr)	Gas Flow: (sccm)
1)	Reset –		380		
2)	Status 1 –	10 s	380		
3)	Slow Pump –	15	650	0	
4)	Pump Down 1 –	6	650	0	
5)	Leak Check –	1	650	< 250	
6)	Ramp Up 1 –	40 s	650	300	150 N_2
7)	Heat Up –	15	650	300	150 N_2
8)	Ramp Down 1 –	1	650	1	1 N_2
9)	Pump Down 2 –	2	650	0	
10)	Ramp Up 2 –	40 s	650	300	25 SiH_4
11)	Poly –	~167	650	300	25 SiH_4
12)	Ramp Down 2 –	40 s	380	1	1 SiH_4
13)	Pump Down 3 –	1	380	0	
14)	N_2 Pump 1 –	15 s	380		20 N_2
15)	Ramp Up 3 –	40 s	380		100 N_2
16)	Post Purge –	1.33	380		100 N_2
17)	Pump Down 4 –	1	380	0	
18)	Isolate –	15 s	380		
19)	N_2 Pump 2 –	15 s	380		
20)	Backfill –	10	380		
21)	End –	1 s	380		

Table 3-6: 100 Å Dry Oxide Recipe for Bruce Furnace

Step:		Time: (min)	Temp: (°C)	Gas Flow: (lpm)
1)	Boat Out –		25	5 N_2
2)	Start –	1 s	800	10 N_2
3)	Push In –	12	800	10 N_2
4)	Stabilize –	20	800	10 N_2
5)	Ramp Up –	20	900	5 N_2
6)	Stabilize –	5	900	5 N_2
7)	Soak –	13	900	10 O_2
8)	N_2 Purge –	5	25	15 N_2
9)	Ramp Down –	35	25	10 N_2

Table 3-7: 1000 Å Stoichiometric Nitride Recipe for ASM LPCVD

Step:		Time: (min)	Temp: (°C)	Pressure: (mTorr)	Gas Flow: (sccm)
1)	Reset –		380		
2)	Status 1 –	10 s	380		
3)	Slow Pump –	15	800	0	
4)	Pump Down 1 –	6	800	0	
5)	Leak Check –	1	800	< 250	
6)	Ramp Up 1 –	40 s	800	300	150 N_2
7)	Heat Up –	20	800	300	150 N_2
8)	Ramp Down 1 –	1	800	1	1 N_2
9)	Pump Down 2 –	2	800	0	
10)	Ramp Up 2 –	40 s	800	300	20 SiH_2Cl_2 & 50 NH_3
11)	Nitride –	~55	800	300	20 SiH_2Cl_2 & 50 NH_3
12)	Ramp Down 2 –	40 s	380	1	1 SiH_2Cl_2 & 1 NH_3
13)	Pump Down 3 –	1	380	0	
14)	N_2 Pump 1 –	15 s	380		20 N_2
15)	Ramp Up 3 –	40 s	380		150 N_2
16)	Post Purge –	10	380		150 N_2
17)	Pump Down 4 –	1	380	0	
18)	Isolate –	15 s	380		
19)	N_2 Pump 2 –	15 s	380		
20)	Backfill –	10	380		
21)	End –	1 s	380		

In order to make the piezoresistive polysilicon layer conductive the layer is doped by spinning on Borofilm 100 with an SCS P6700 spinner at 2000 RPM. The Borofilm is not as thick as the AZ9260 and thus does not coat the wafers as thickly, leaving radial coating streaks outwards from the plateaus. This appears to not be a problem as the top of the plateaus received at least a moderate coating of Borofilm as the resistors proved resistive in later testing. A 20 minute bake in a conventional oven (air environment) at 200 °C drives the solvents out of the Borofilm before the diffusion step. A short, 900 °C drive-in in the Bruce Furnace dopes the polysilicon (Table 3-9).

Table 3-8: 1000 Å Polysilicon Recipe for ASM LPCVD

Step:		Time: (min)	Temp: (°C)	Pressure: (mTorr)	Gas Flow: (sccm)
1)	Reset –		380		
2)	Status 1 –	10 s	380		
3)	Slow Pump –	15	610	0	
4)	Pump Down 1 –	6	610	0	
5)	Leak Check –	1	610	< 250	
6)	Ramp Up 1 –	40 s	610	300	150 N_2
7)	Heat Up –	15	610	300	150 N_2
8)	Ramp Down 1 –	1	610	1	1 N_2
9)	Pump Down 2 –	2	610	0	
10)	Ramp Up 2 –	40 s	610	300	25 SiH_4
11)	Poly –	~13	610	300	25 SiH_4
12)	Ramp Down 2 –	40 s	380	1	1 SiH_4
13)	Pump Down 3 –	1	380	0	
14)	N_2 Pump 1 –	15 s	380		20 N_2
15)	Ramp Up 3 –	40 s	380		100 N_2
16)	Post Purge –	1.33	380		100 N_2
17)	Pump Down 4 –	1	380	0	
18)	Isolate –	15 s	380		
19)	N_2 Pump 2 –	15 s	380		
20)	Backfill –	10	380		
21)	End –	1 s	380		

900 °C was used as the diffusion temperature because it correlated roughly with the maximum gauge factor predicted for P-type polysilicon while providing sufficiently fast diffusion rates. The maximum gauge factor occurs near a doping of 1E19 cm^{-3} as shown in Figure 3-9 (a) [32]. Figure 3-9 (b) indicates this doping level could be achieved by saturating the polysilicon to boron's solid solubility at about 650 °C [33]. However, based on the trend of Figure 3-9 (c), diffusion rates at this temperature are slow and impractical [33]. Long diffusion times need to be avoided so the polysilicon is not consumed in oxidation, due to oxygen diffusing from the Borofilm. With this process, Figure 3-9 predicts a doping concentration of

1E20 cm^{-1}. With the doping completed, the Borofilm was stripped in 5.2:1 BOE for about 5 minutes. The doping effects were verified by a 4-point resistance probe.

Table 3-9: 900 °C Spike for Bruce Furnace

Step:	Time: (min)	Temp: (°C)	Gas Flow: (lpm)
1) Boat Out –		25	5 N_2
2) Start –	1 s	900	10 N_2
3) Warm Up –	45	900	10 N_2
4) Push In –	12	900	10 N_2

Note: Push In takes less than 12 minutes so the wafers sit in the tube for roughly 8 min.

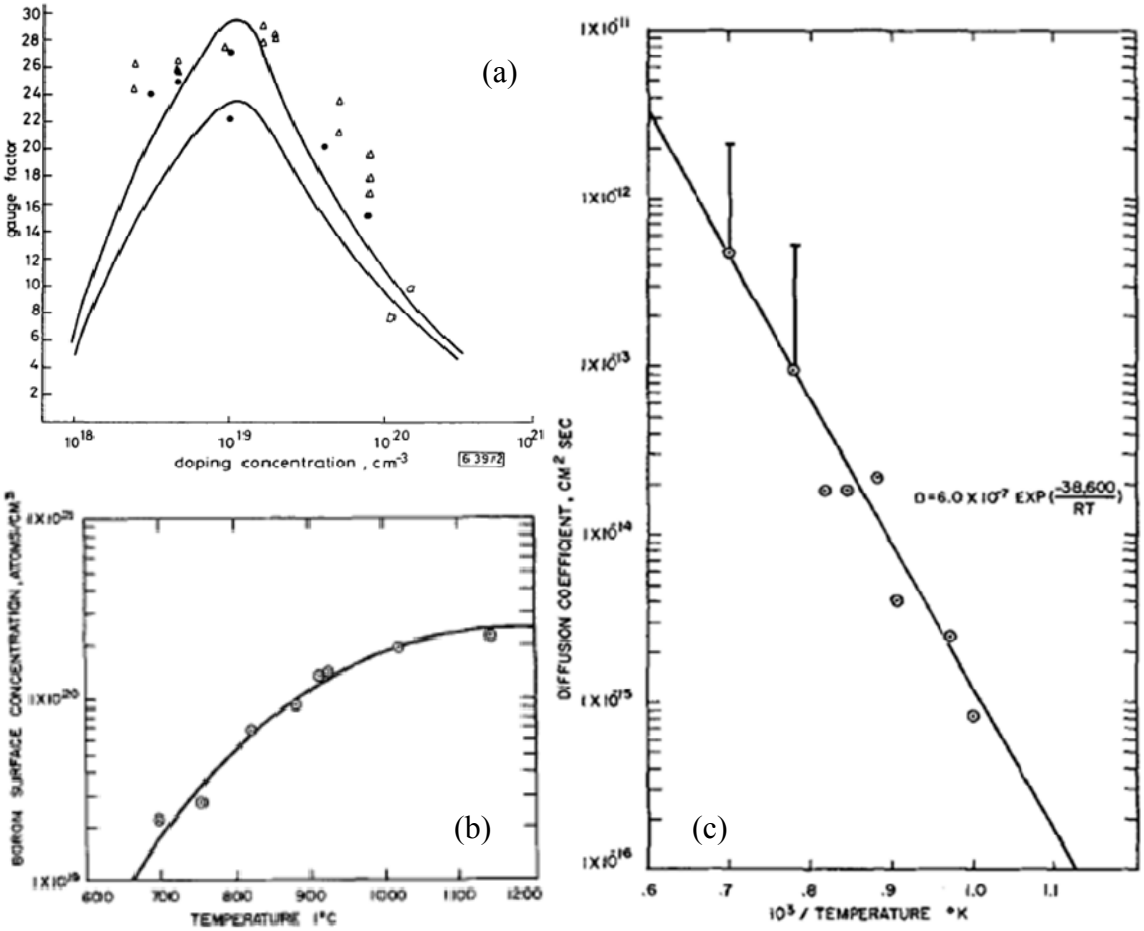


Figure 3-9: (a) Effect of dopant concentration on piezoresistive gauge factor in P-type polysilicon. Curves represent minimum and maximum predicted value based on two variations of a model. Data points represent experimental data on piezoresistive gauge factor in P-type polysilicon. (Reproduced with permission [32].) (b) Solid solubility of boron in single crystal silicon based on temperature and (c) diffusion coefficient based on temperature. (Reproduced with permission of ECS – The Electro Chemical Society, [33].)

3.8 Piezoresistor Lithography

Two separate masks were used to define the piezoresistive features through a double-exposure, double-develop process:

1) Initially the wafer was coated with photoresist according to the process mentioned in Section 3.4.1.
2) Then the first mask, which masks off the region around the piezoresistor features, allowed for the majority of the photoresist to be exposed with the standard dosage of 1440 mJ/cm^2.
3) The majority of the photoresist is then developed off, again judging the endpoint by the disappearance of the cloudy photoresist. It is acceptable to remove the wafer from the developer when some of the cloudy photoresist is still on the wafer as it will be developed off in the next develop step.
4) The wafer is rinsed and dried as usual.
5) Then the second mask is used to define the actual piezoresistive features in the remaining photoresist left around the features. The exposure dosage this time is 1/3 of the original, 480 mJ/cm^2.
6) Then the wafer is developed again. The develop time in this step is shorter and it is important to agitate the bath in order to get the developer into the crevices of the features, such as the interior of the Picture Frame. It appeared to take about 2/3 of the standard development time and requires observations in a microscope to ensure completion. Because the photoresist is still photosensitive it is important to not look at any feature for too long as it will become exposed and develop off if additional developing is required.
7) Rinse and dry the wafer.

This process is important because of the discrepancy in exposure and development times for features on and off plateau. Because the PR on top of the plateau is only 4 μm thick, in comparison to the 12 μm thickness over the general wafer, it only requires ~1/3 of the exposure and development time.

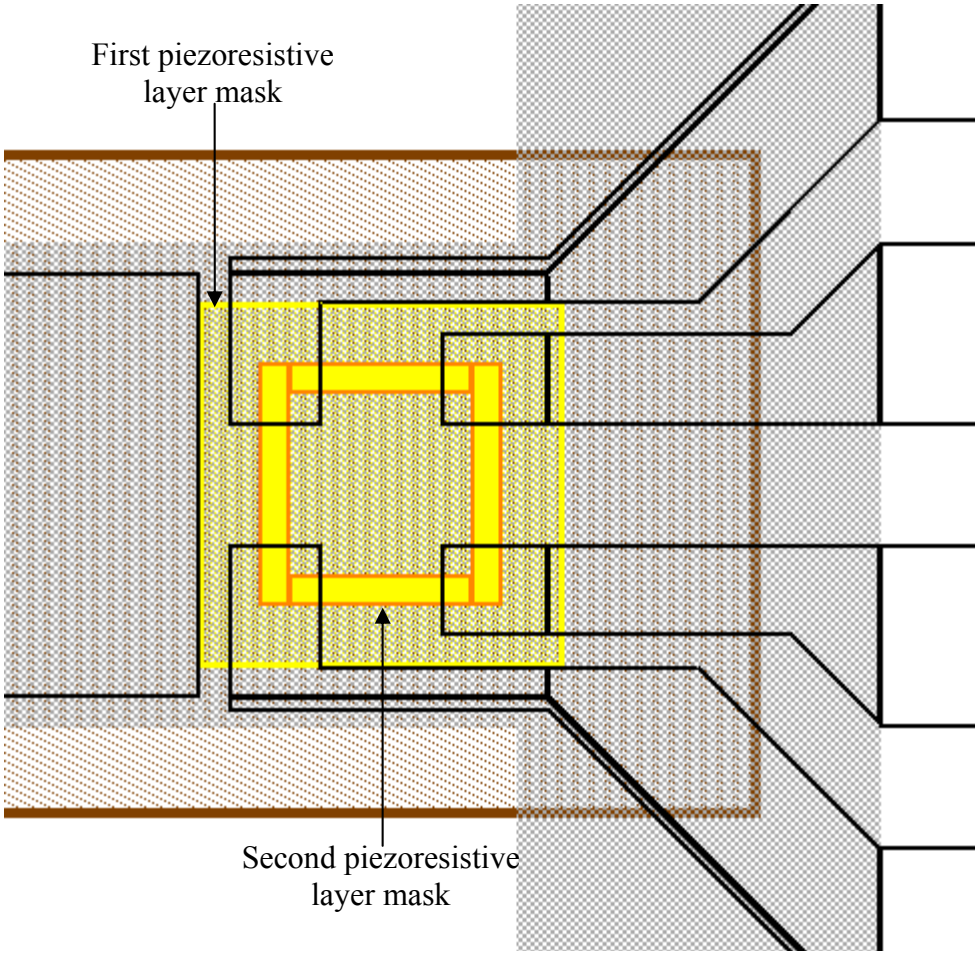


Figure 3-10: The lightly shaded yellow region represents the first exposure mask in the piezoresistor lithography process. The solid yellow region with orange outline is the actual piezoresistor that will be defined by the second exposure mask in the PR left by the first exposure and development stage.

In order to make the features broader and harden it to withstand the RIE etch, the PR is hard baked at 125 °C for 3 minutes. Then a polysilicon etch process is executed in the Drytek Quad with the same 5 minute O_2 clean and 5 minute seasoning run of the recipe on each carrier. The recipe used was 40 sccm SF_6, 50 sccm O_2, 150 mTorr chamber pressure, and 200 W of RF power (chamber 1).

The endpoint of the piezoresistive etch is monitored by optical endpoint detection using Spectra Suite software and Ocean Optics hardware. In order to get

an idea of the endpoint conditions that could be expected in the RIE etches, the backside of a few of the wafers were etched and their optical response at 705.2 nm was monitored (Figure 3-11). For the piezoresistor etch, it was decided to etch until the signal to drop off indicating that all of the doped polysilicon was removed (took a little over a minute on average).

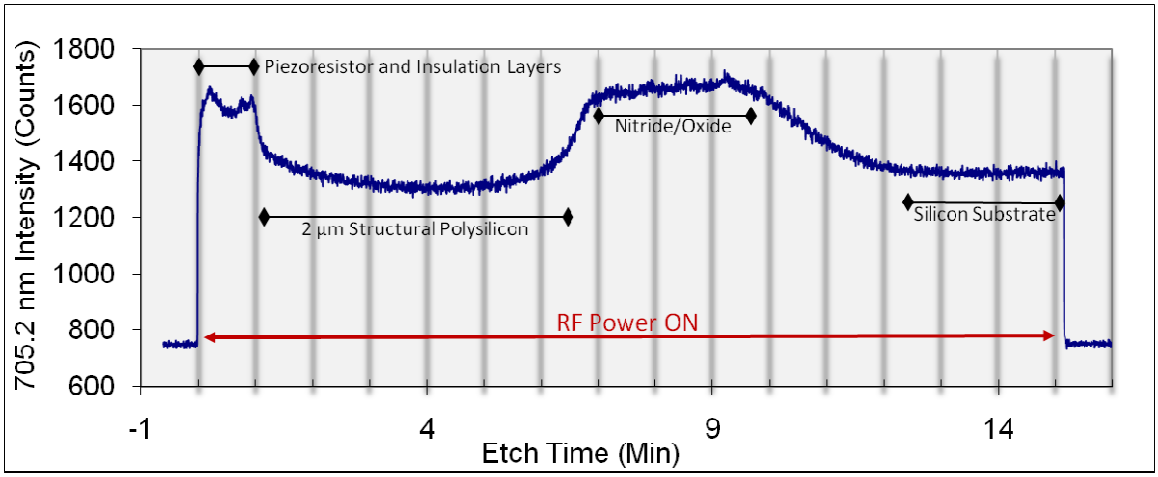


Figure 3-11: Optical endpoint signal at 705.2 nm for backside of one wafer in polysilicon etch recipe.

3.9 Cantilever and Support Structure Definition

Figure 3-11 shows that roughly 7 to 8 minutes would be sufficient to etch through the structural polysilicon layer and partially into the oxide layer used to form the balloon cavity. To verify this time on each wafer the etch was stopped when the endpoint signal was roughly 2 minutes into the nitride/oxide region in Figure 3-11. This resulted in a ~3500 Å oxide layer. A 0.5 µm aluminum hard mask was used to withstand the 8 minute etch. The reflective nature of the aluminum coating appeared to over-expose the photoresist so the dosage was dropped by 1/3 to 960 mJ/cm^2.

3.10 Aluminum Interconnect Definition

Sputtering of the aluminum was done the same way as before with an SC2 clean first. A short, ~30 s, submersion in 5.2:1 BOE immediately before going into the sputtering chamber removed the native oxide to improve the electrical interface. Again, the lithography was problematic because the feature size on top of the plateaus was a minimum of 5 μm. This time the feature size was increased to 7.5 μm to account for the over-exposure and over-development. Although successful samples were obtained, no exposure dose proved reliable due to process variation.

The aluminum PR features were hard baked at 125 °C for 3 minutes to broaden the features, making them more pronounced. Then the pattern was transferred into the aluminum with the aluminum etch. The wafer was sintered in the P-type doping tube of the Bruce Furnace according to the following recipe:

Table 3-10: 450 °C Sinter Recipe for Bruce Furnace

Step:	Time: (min)	Temp: (°C)	Gas Flow: (lpm)
1) Boat Out –		25	5 N_2
2) Start –	1 s	450	10 N_2
3) Warm Up –	30	450	10 N_2
4) Push In –	30	450	10 N_2
5) Stabilize –	15	450	10 H_2/N_2
6) Soak –	15	450	5 H_2/N_2
7) N_2 Purge –	5	450	10 N_2
8) Pull Out –	15	25	5 N_2

3.11 Mold Cavity Definition

Lithography defines the access holes of the mold cavity in photoresist. The PR was hard baked at 140 °C for 5 minutes to harden it for the etch. A 5 minute aluminum etch opened access holes in regions where the pneumatic interconnect

overlapped the electrical interconnect. At this point, the wafer was diced to decrease the time required to etch the mold cavity in XeF_2. A K&S (Kulicke & Soffa) 775 wafer saw was used, and the photoresist and the features defined in it were protected by placing a piece of the wafer mounting tape over the front of the wafer during dicing. After dicing, the dice were well rinsed and washed in a bath of room temperature water with WRS 200 cleaning solution. The tape protecting the front side was left on through this in order to keep particles from being washed into the small windows of the mold access holes. The dice were etched in a Drytek Quad unit with 100 sccm of CF_4, 20 sccm of O_2, 200 mTorr chamber pressure, and 225 W for 15 minutes. (Note: This recipe was used in chamber 3 that commonly reports a weaker RF output than specified in the recipe.)

Once the oxide mask was formed, the sides and the bottom of the wafer were protected by painting photoresist on with a Q-tip. The photoresist was baked at 140 °C for 3 minutes in a proximity bake, to keep the PR from sticking to the hotplate, by resting the die on a paper clip unfolded to serve as a platter. The mold-patterned photoresist remains on the die to protect the substrate and the features built on it (cantilever, support structure, and piezoresistor) from being etched in the XeF_2. This not only ensures that the device will not be destroyed but also enhances the etch rate of the balloon cavity by limiting how much silicon the XeF_2 can etch.

The XeF_2 etcher, by Xactix, etched each die with 50 pulses of 2 Torr XeF_2 for 2 minutes per pulse. This produced a lateral etch in excess of 100 μm around all of the balloon and microchannel features (Figure 3-12). To remove the photoresist

without damaging the oxide mold the dice were etched (ashed) in the O_2 clean recipe used for cleaning out the chamber. This was done for up to an hour; however, some photoresist appeared to remain even after this time.

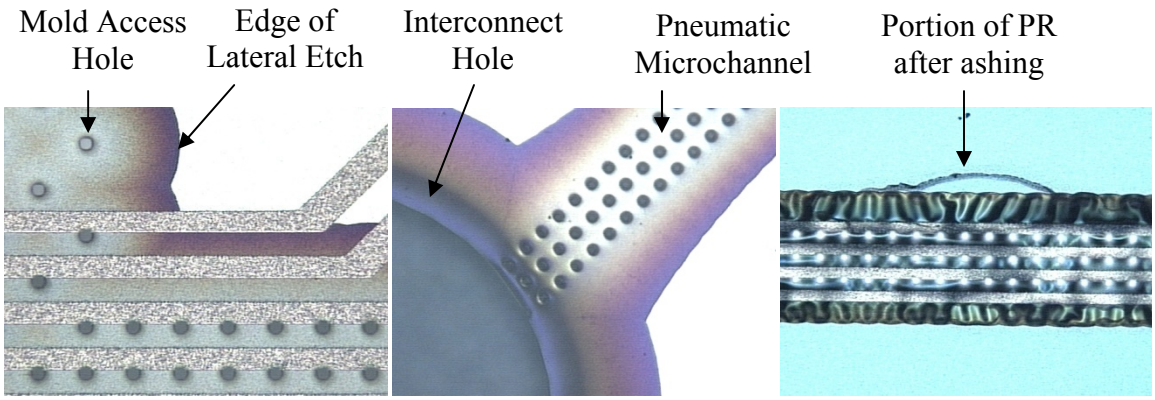


Figure 3-12: Edge of balloon feature with aluminum and microchannel interconnect coming in from the right (Left, 20x) and interconnect access hole for external air pressure and microchannel leading off to the top-right (Center, 10x) after the XeF2 etch. Remnants of photoresist after ashing over microchannel (Right, 10x)

3.12 Balloon Deposition

To prepare the dice for Parylene they were vapor primed, overnight, with A-174 silane adhesion promoter. Then the wafers received a ~10 μm Parylene coating in an SCS PDS 2010 by dispensing 13 grams of the Parylene dimer into the furnace. The dice were placed on top of a paper clip in order to simplify removal from the machine after the deposition.

3.13 Cantilever Release

The lithography process was performed and the release pattern was transferred into the Parylene by RIE using the O_2 clean, 'ash,' recipe for 10 minutes. Then the die was dipped in BOE. The Parylene was able to sustain itself in the BOE for over 4 hours; however, it was significantly (hundreds of micron) underetched by

the BOE attacking the thermal oxide of the mold cavity (Figure 3-13). The aluminum interconnect was attacked by the BOE and the devices became useless. Additionally, the ashing of the Parylene to create the mask opened up the access holes in the mold, effectively destroying the balloon membrane (Figure 3-14). Photoresist could not be used as a mask as it flaked off after two hours in the BOE (Figure 3-13).

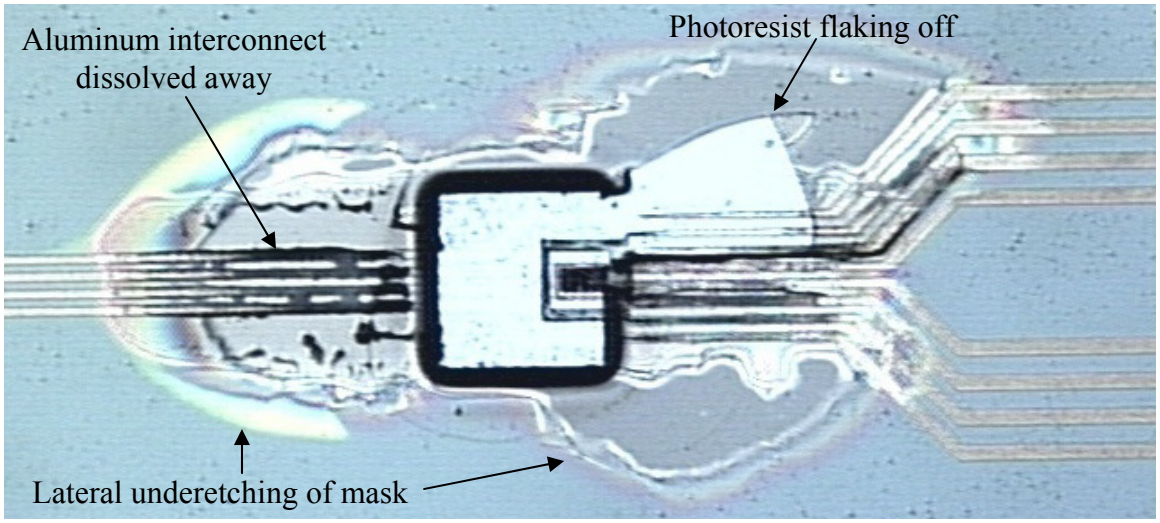


Figure 3-13: The square is the region exposed by the lithography step; the top right section of photoresist flaked off after 2 hours in 5.2:1 BOE. The oxide layer used for the mold cavity was also attacked by the BOE and accounts for the rings around the device and interconnect.

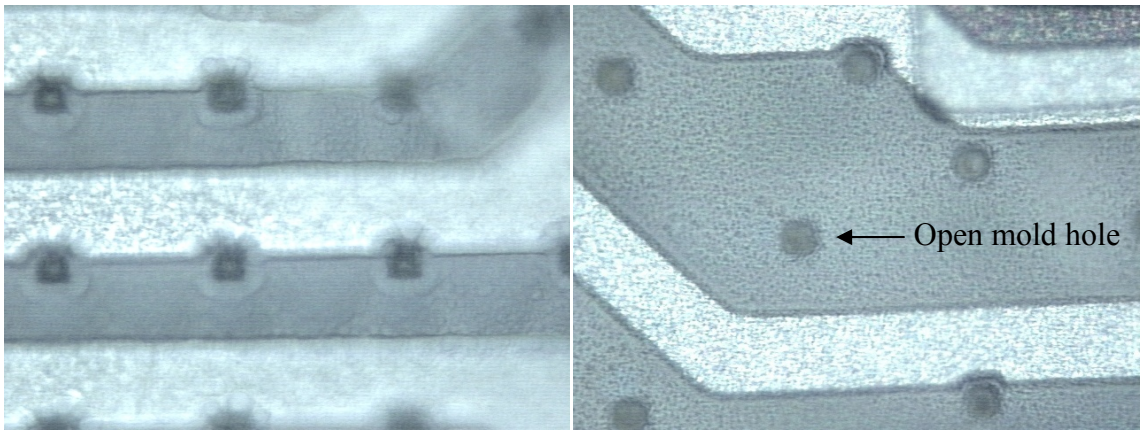


Figure 3-14: Properly sealed balloon membrane holes, evident from shiny reflection in center, after Parylene deposition (Left). These access holes have been reopened in some cases due to ashing step used to form release mask (Right). (50x)

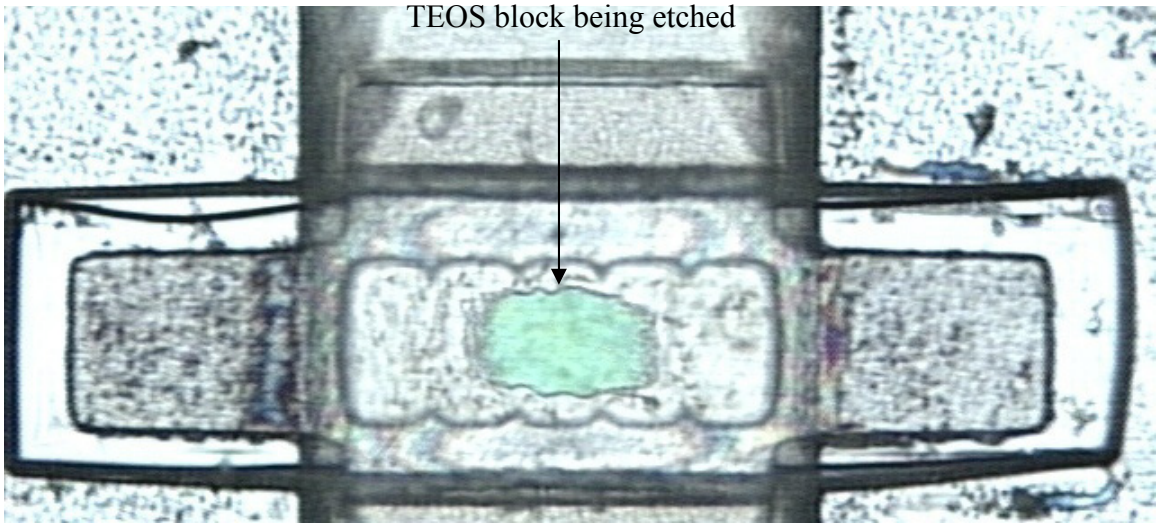


Figure 3-15: Release test structure after 4 hours in 5.2:1 BOE. The window shows a chunk of TEOS being etched from all directions, suggesting that the polysilicon structure has lifted off due to underetching of the thermal oxide used for the balloon mold. (20x)

As further evidence of the etching of the thermal oxide and a further consequence of the its absence, the release test structure shows that the TEOS in the windows was being attacked from all sides, not just the open ends of the structure. The circular shape of the TEOS in the observation windows of the polysilicon, Figure 3-15, points to the fact that the BOE had access to it from the top and bottom of the picture also. This could only happen when the thermal oxide below the polysilicon supports was etched away and the polysilicon structure was floating. Therefore, the actual devices will also be lifted off and will be useless as they could be brushed away by contact with anything.

4 Results & Discussion

4.1 Lithography

One of the challenges in this fabrication process was the lithography process. There were large discrepancies encountered from the large topography and from the variation in photoresist processing. The piezoresistor level achieved more repeatable and desirable results by utilizing a double-exposure, double-develop process, and the aluminum level should receive this same processing. In order to make this process effective, it is necessary to not only protect photoresist for features to be defined on the plateaus, but also to give a border around features off the plateau. This border improves the definition of off plateau features by allowing for misalignment and accounting for the small band of photoresist lost during the second exposure and develop. For instance, the alignment crosshairs in the piezoresistor's first mask were expanded by an extra 2.5 μm in each direction. This may have been sufficient, but a more detailed analysis of the features may lead to a need for a larger margin around the features. However, if this margin becomes too big the additional development time required to define the features on top of the plateau will be insufficient to develop the margin away and will lead to the original problem.

Furthermore, the alignment crosshairs for the later levels could be made slightly larger, as their current width of 10 μm tended to be etched or developed away. Additionally, it was found that the alignment crosshairs used for the

sacrificial level, which were made to the same size as the encompassing marks, were easier to align to than the later alignment marks, inset by 5 μm (Figure 3-4).

As an interesting side note, it was observed that the hard baking of exposed photoresist caused distortion of the photoresist. As the dice were examined after development, to ensure full opening of the photoresist windows, the photoresist became exposed in some areas due to prolonged observation under the unfiltered microscopes. When the features were deemed acceptable they were hard baked in preparation for RIE etching or other process, but the exposed PR bubbled up in the exposed areas, as shown in Figure 4-1. Higher temperatures and longer times appeared to make final distortion worse, but even the shortest and coolest hard bakes caused some distortion.

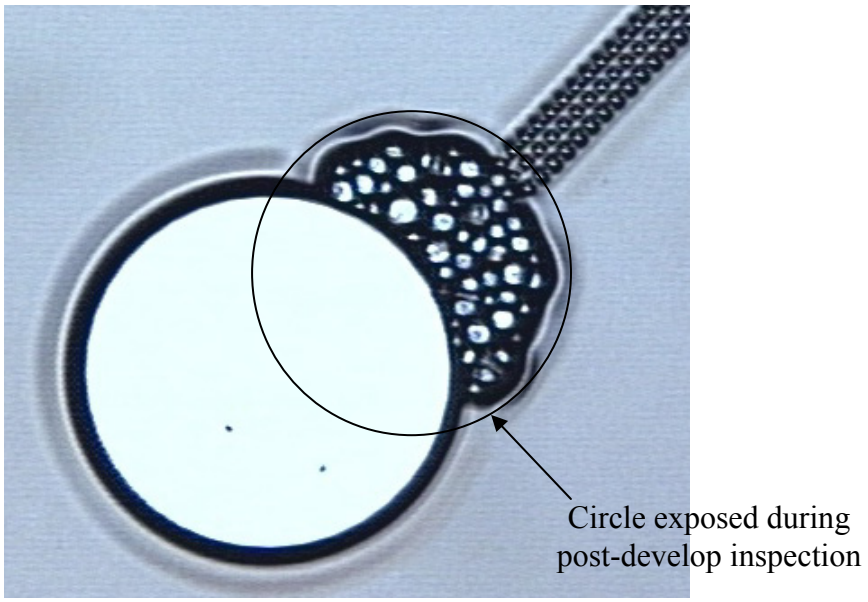


Figure 4-1: Photoresist distortion caused by hard baking after photoresist exposed during post-development inspection. Notice the bubbles form a partial circle centered around the edge of the interconnect access hole where the microchannel meets it and where the microscope was inspecting.

4.2 Piezoresistor Definition

With the double-mask lithography process all of the piezoresistor layouts resolved as designed, with the exception of the unsupported design. All instances of the unsupported design produced significantly undersized results and, in many cases, gaps along their length as in Figure 4-2. This is due to the insufficient margin surrounding the patterns. To ensure that the gap between the resistors was defined, very little area was blocked off in the initial mask layer (Figure 4-3). Therefore, increasing the margin of protection around these features and protecting the space between them should improve their resolution.

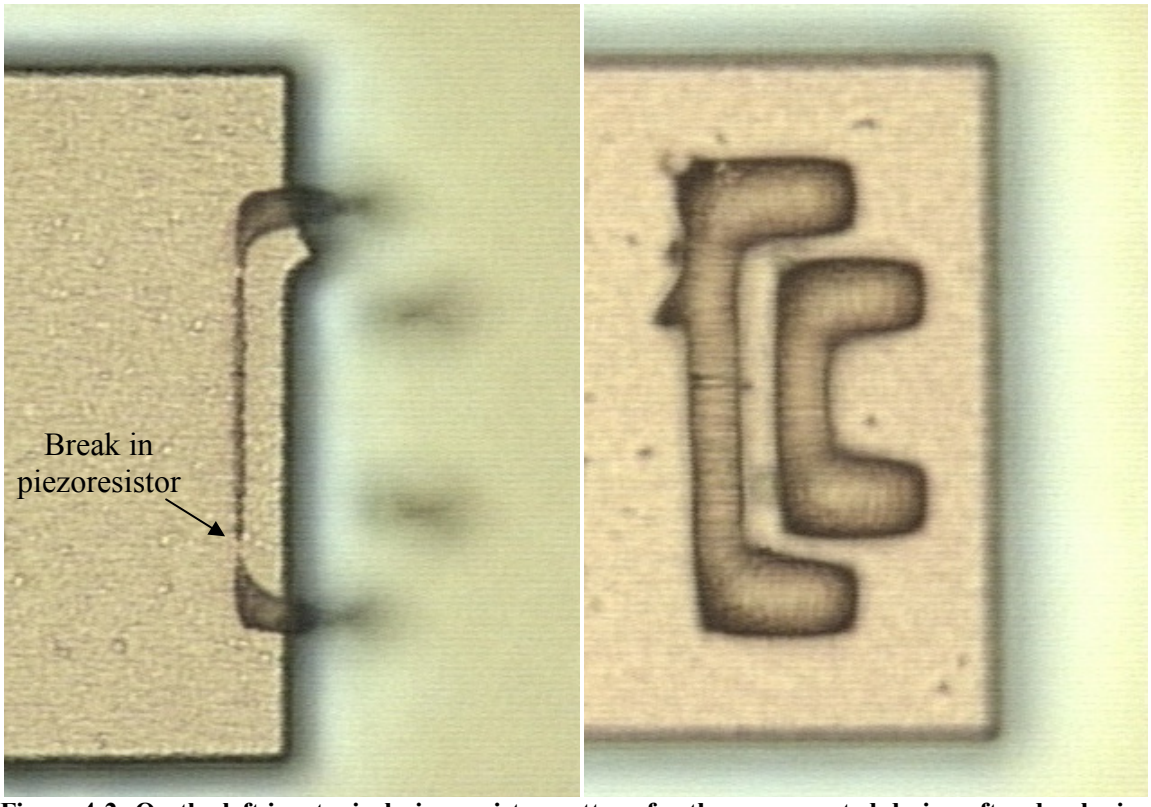


Figure 4-2: On the left is a typical piezoresistor pattern for the unsupported design after developing and hard baking; the smaller, right resistor is out of focus as it is off the plateau, but is analogous to the larger, left resistor. The features should have appeared roughly as they did in the basic design (right) except shifted to the edge of the plateau. (50x)

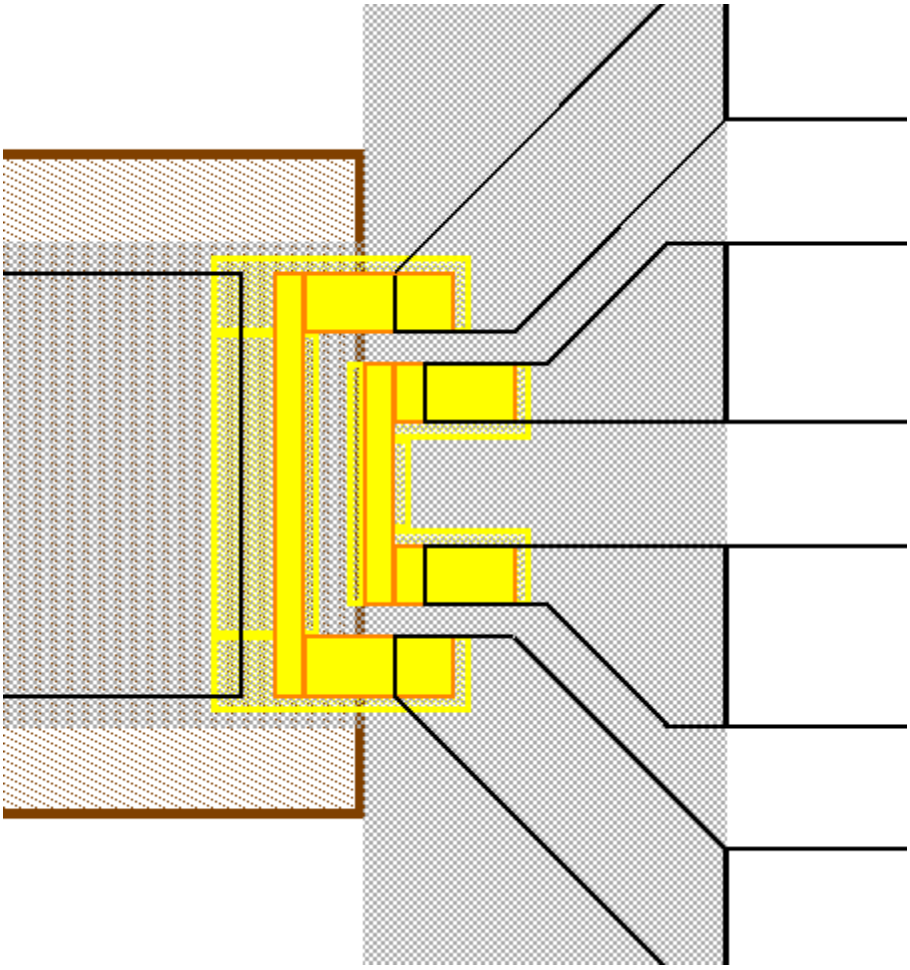


Figure 4-3: The current first level of the piezoresistor lithography step (hashed yellow with yellow outline) is insufficient to protect the final piezoresistor level features during the dual exposure and develop lithography.

4.3 Substrate Choice

During processing it became apparent that the choice of 100 mm wafers was not optimal. Because the majority of machines available are designed to work with 150 mm wafers, carriers had to be used to hold the device wafers during many of the processing steps involved in fabrication. The carriers introduce a number of negative side effects. First, the device wafer sits in a recessed pocket on the carrier, but this recess is not deep enough to allow the device to sit flush with the carrier's surface. Therefore, the wafer is actually closer to the electrodes of RIE systems.

Second, there is a gap between the wafers that causes poor thermal conductivity between the device wafer and the bottom electrode (may be temperature controlled) of some machines. Third, the gap also introduces a change in the capacitance of the two electrodes that may be significant because of the high frequency RF energy being applied to the capacitor formed by the electrodes of RIE systems. Fourth, the carrier is a source of interference. When observing optical endpoint profiles the signal created by the material being etched may be obscured by the signal created from etching of the carrier. Fifth, etching of the carrier will consume some of the etchants otherwise available to etch the device. All of these effects can have a significant impact on the process by changing etch rates, etch uniformity, film deposition rates, film properties, etc. Therefore, it is always best to work with the size substrate the processing systems are meant and tuned to handle.

4.4 Mold Cavity Material

As mentioned in the Cantilever Release Section (3.13), at least a portion of the device's failure was caused by the choice of material for the balloon cavity. Because the BOE also attacked the thermal oxide of the mold, it attacked the aluminum interconnect and most likely lifted off the polysilicon structure defined on the oxide. The oxide was originally chosen as the mold material to be compatible with the fabrication of the microhand. However, it is known that the etch rate of nitride in XeF_2 is almost as slow as oxide's; therefore nitride could probably be used instead of oxide. This is beneficial because it will not be attacked by the BOE during release; allowing the cantilever structure to stay adhered to the balloon and

preventing the aluminum interconnect from being exposed to the BOE. Furthermore, because the nitride is more resistant to the BOE it should also improve the resiliency of the Parylene's interface to the mold cavity, further decreasing the underetching. Additionally, the use of nitride will save on a process step, as the first thermal oxidation will not be needed; the initial LPCVD nitride step will just have to be thicker. It was also noted that the composition of the nitride is important to keep its etch rate low, in BOE and XeF_2. Therefore, a stoichiometric nitride may be the best choice for this layer. Unfortunately, nitride usually cannot be deposited directly on silicon and thus further research will be required to find a solution. One possible solution would be to use PEVCD nitride that can be deposited on silicon, but does not hold up in BOE, and change the sacrificial and cantilever materials.

4.5 Considerations of Different Sacrificial and Cantilever Materials

Due to the complications involved in the release step, another possibility may be to consider alternative materials to use as the sacrificial layer. This would involve considering a different material for the cantilever in order to ensure that it is not etched by the new release step. One possibility would be to use polysilicon as the sacrificial material and either oxide or nitride for the cantilever. Then XeF_2 could be used as the release agent.

The advantages to this approach are that there have been promising results shown in this work with silicon and XeF_2 and it is a dry step so problems of stiction can easily be avoided. Additionally, because the cantilever is already an insulator the reoxidation and nitride steps could be skipped before forming the piezoresistor

layer. The XeF_2 etch process can be monitored as it is occurring so the endpoint may also be easier to observe, although the current microscope available for the task has insufficient magnification to observe the small windows of the release structure.

However, formation of an 8 μm polysilicon layer is unrealistic. That was the main advantage of TEOS – it has low stress and fast deposition rates. Potentially, a thinner sacrificial layer could be used at the cost of sensing range or the device could be scaled down, as is required for use with the microhand under development.

4.6 Release Mask

The release mask needs improvement. A large area around the access point of the BOE can improve the diffusion of the BOE into the access holes, decreasing etch time. On the other hand, the fact that BOE attacks aluminum and that the aluminum interconnect passes through the release windows was forgotten. Therefore, the mask allowed BOE to attack the interconnect running to the second set of piezoresistors as demonstrated in Figure 4-5. This problem is significant but easy to fix by creating a new mask. The mask should open up a more limited area well inside of the aluminum interconnect so that aluminum is completely encased in the Parylene. This may limit the ability of the etchant to get under the cantilever but it is important to protect the interconnect.

Additionally, further consideration should be given to leaving a portion of the sacrificial layer behind as a fulcrum. In order to get a straight fulcrum the underetch must be significant, thus requiring a long time in the BOE, which may be impractical.

Finally, the mask needs to protect the mold holes from being reopened during the ash to open up the window for the release step and the aluminum interconnect pads should be exposed for later wire bonding. To protect them during the release etch, photoresist can be painted on due to the large size of the area and its remoteness from the tiny windows of the release mask.

An example of an appropriate mask can be seen in Figure 4-4. The under etch in this example has been decreased to 50 μm, but this could be decreased further, by extending the window closer to the support structure. One advantage of etching the mask into the Parylene is built-in protection for the top of the cantilever. Because there is a thinner layer of photoresist over the top of the cantilever and Parylene and photoresist etch at about the same rate, the Parylene on the cantilever will be thinned down, but not completely removed by the appropriate etch time to open up the release window. This should leave about a 2 μm layer of Parylene on top of the cantilever that should protect the cantilever and its surface layers from the release agent while minimizing any strengthening of the beam, which would serve to change sensor sensitivity. The disadvantage to this plan is the fact that the aluminum electrodes for signal and chemical sensing (on the longitudinal design) will be covered and useless. On the other hand if they were not covered, they would be etched away in the BOE release. Therefore, the only way to get access to them is to use a different release agent, like the XeF_2, or perform a short post-release ash to remove the top layer of Parylene on the cantilever.

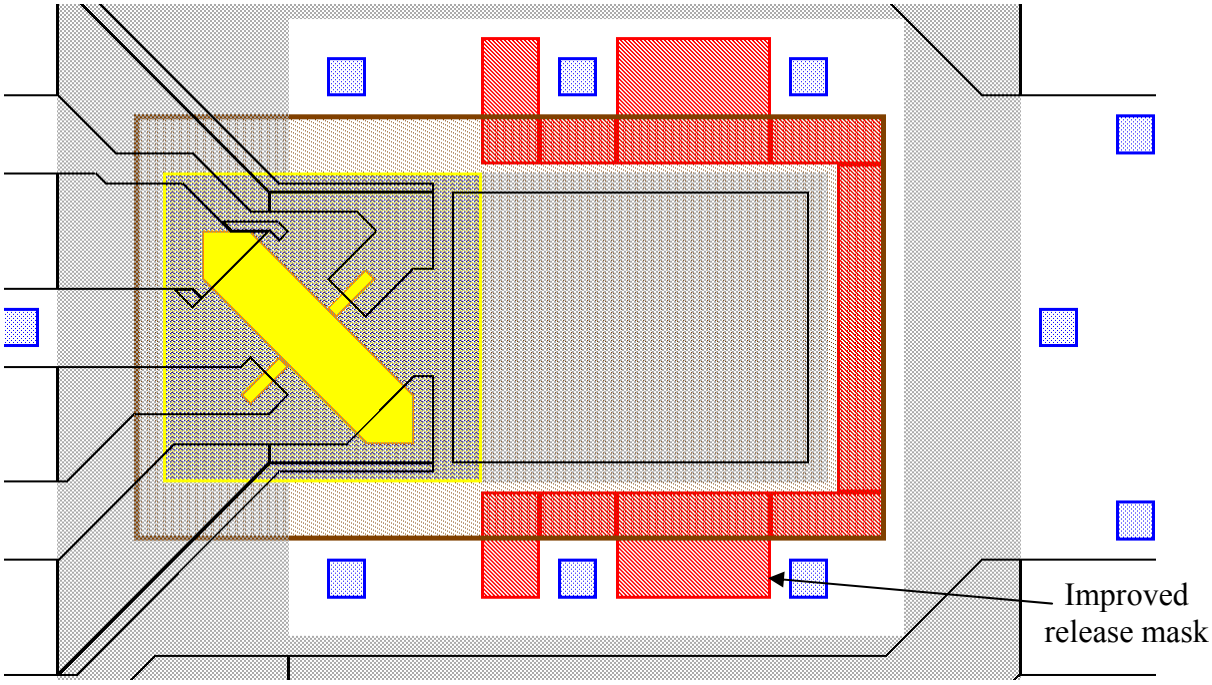


Figure 4-4: Improved release mask design. Red hashed region represents the window to be opened in Parylene as the mask for the release step.

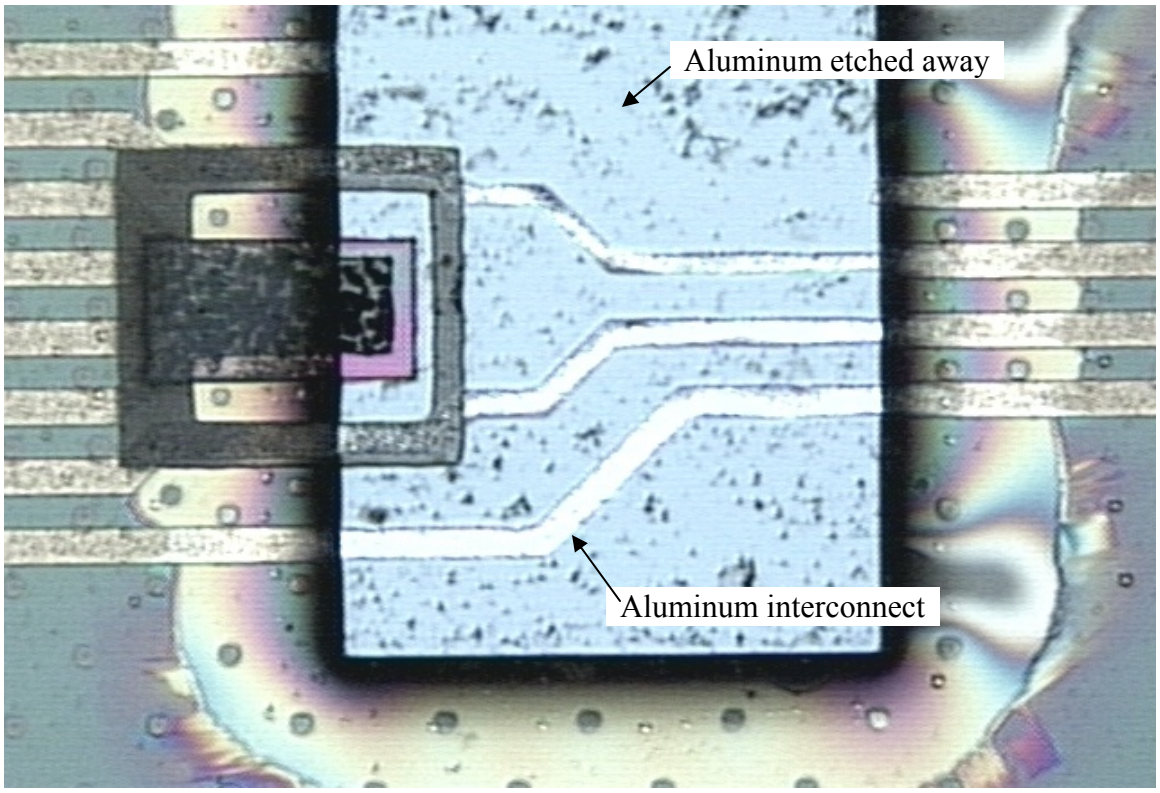


Figure 4-5: One aluminum interconnect line has already been etched away and the others have been considerably shrunk after 1 hour in 5.2:1 BOE. (10x)

4.7 Mold Mask

The access holes created for the mold cavity are larger than they need to be. After observing the holes generated in the oxide, about 12 μm, it became apparent that smaller holes may be useful. The smaller holes require less Parylene to seal them. The disadvantage with that option is that a thinner Parylene coating may be insufficient to act as a balloon and maintain structural integrity when inflated. This will certainly be an option, though, when the device is scaled down for integration with the microhand. Additionally, it was noted that, inconsistently, the size of the access holes within the support structure ring became smaller (~6 μm) after hard baking. This is caused by the reflowing of the photoresist as the PR flowed down off the plateau and filled in the valley formed inside of the support structure ring by the polysilicon. However, the inconsistency refers to the fact that this was only observed on one of the wafers and others did not exhibit it. The reason for this discontinuity is not known, but probably relates to how the photoresist was hard baked.

4.8 Test Plan

During different steps of fabrication and inspection it became apparent that using the profilometers available would be difficult due to the large stylus size (~10 μm with a 45° shank) and the inadequate optics. Without a more narrow and sharp stylus it would be difficult to land the tip near the end of the cantilever as desired for the test. Again, the optics would make it difficult to determine where the stylus was actually landing. Additionally, it would be difficult to see if the cantilever

is actually being deflected when the stylus pushes down on it. These are important considerations for testing and alternatives should be investigated.

5 Conclusion and Future Work

5.1 Conclusion

The majority of process steps were completed to satisfaction after some experimentation was completed. However, the final step failed in its ability to release the cantilever because the release agent attacked significantly more than desired. All of the devices were rendered useless because of this. As a result, none of the theoretical designs and functionality could be tested. Once the suggested improvements are made, it should be possible to create usable and testable devices.

5.2 Future Work

The next steps in this project are to apply and test the recommendations made in the Results & Discussion Chapter: create two new masks (one for the first stage aluminum and the other for the release level), repeat the fabrication process with the new masks and a nitride balloon mold. To save time it is advisable to first test the nitride layer in XeF_2 to ensure that it is of sufficient quality to hold up against the etchant. This can be best achieved by patterning the nitride with oxide mold and etching the mold cavity. Then Parylene can be deposited on the surface, patterned with the release mask, and soaked in BOE. If the Parylene indicated no signs of losing its hold, it is reasonable to assume that the change in the fabrication process will yield a functioning device. If not, other ideas will have to be considered, including alternative sacrificial and cantilever materials, as well as fresh adhesion promoter. Other recommendations made in the chapter could then be attempted.

The key to successful fabrication may be creating a more effective and repeatable lithography process. Using a different developer, such as AZ 400K, or fresh AZ9260 may be good starting points.

With functional devices, testing becomes important to determine the effectiveness of the different variations with the intent of improving the design. Many of the processes (such as RIE and doping) could use further development and refinement to improve device performance, increase yield, decrease processing time, and simplify complexity. Integration with the microhand and a haptic interface system could then be pursued. This alone is a significant task. This would require signal processing, interfacing, software development, and additional hardware. One possible idea would be to integrate some logic systems into the microhand capable of multiplexing the signals and transmitting the data wirelessly. With such an interface, only power and pneumatic pressure would have to be supplied to the microhand. Additionally, the process could be modified to use gold, or some biocompatible conductor, to make the electrical interconnect out of and allow the probe electrodes, on the longitudinal design, to be exposed to the environment. Further refinements to the design could be created by adding resistors that do not experience stress to serve as temperature sensors.

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